RUPRECHT-KARLS-
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Exercise:
CAM - Part 1

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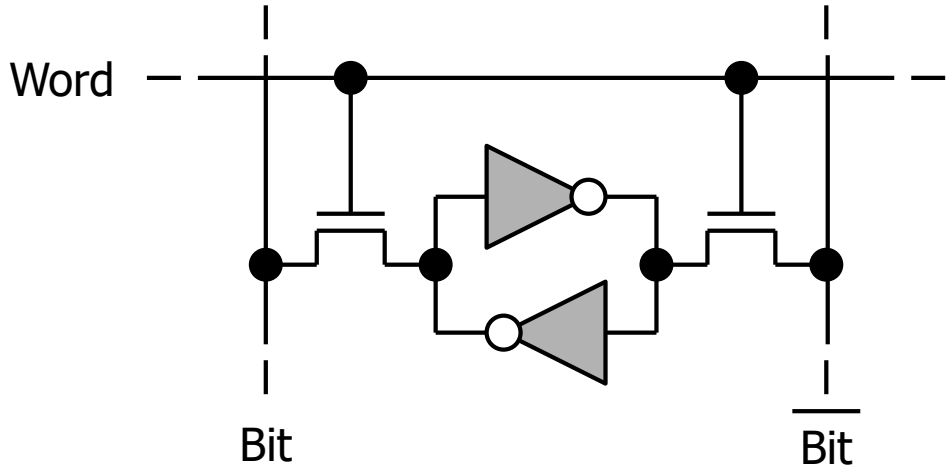
Background

- For an understanding on SRAMs and CAMs, see the lecture slides on the course web page.

SRAM_Cell

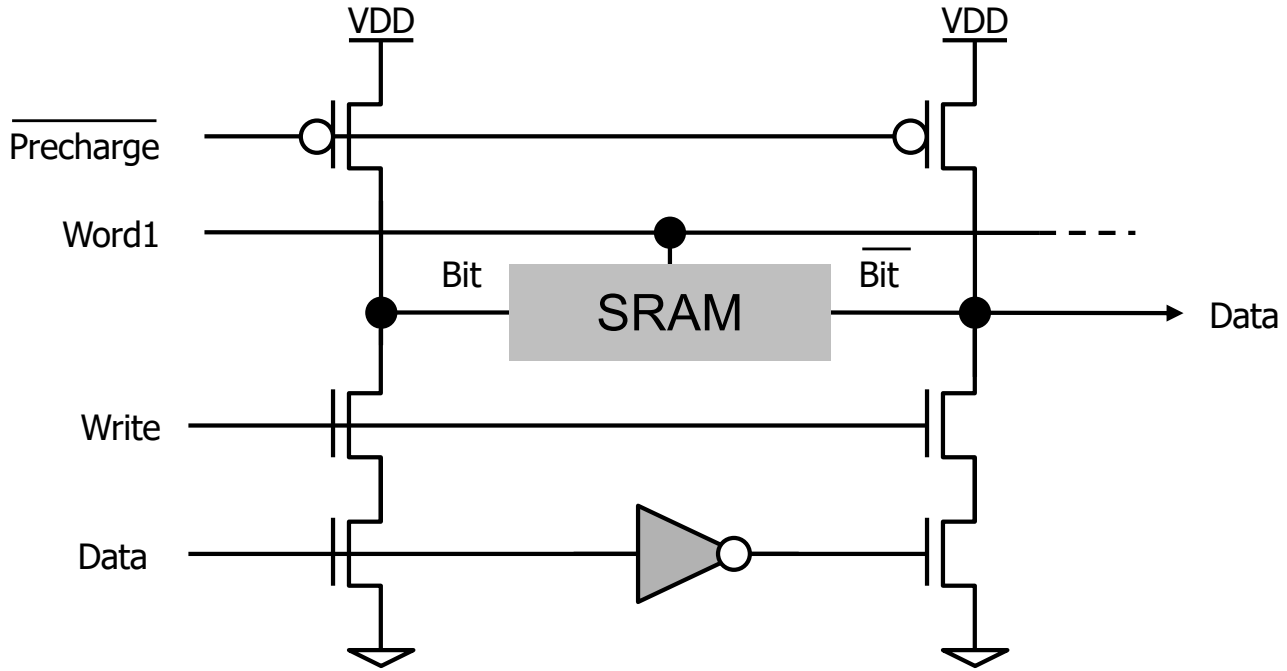
- Create schematic and symbol of a SRAM_cell



- Pins should be: **`Bit, BitB, Word`**
- Use global nets vdd! and gnd! for the supplies
- Use minimal lengths for the NMOS
- Use WNWRITE for the write NMOSs, start with 0.44um
- Use WNINV for the other NMOS, start with 0.44um
- Use WPINV = minimum and LPINV = minimum for the PMOS

Simulating ONE SRAM cell

- Create the following schematic SRAM_SIM



  - Use wide (10 µm), minimum length MOS for driving
  - You can use a VCVS for the inverter (how ? ...)
- Create control signals which
  - Write 0 to the SRAM, then read it back. Then try writing 1.
  - You can create a signal with multiple pulses by stacking vpulses
  - Use for instance 5ns for precharge

Simulating MULTIPLE cell

- Add a second SRAM cell on the same bitlines ('below')
  - You also need a further control signal Word2
- Create signals for the following sequence
  - Write 0 to the first RAM cell
  - Write 1 to the second RAM cell
  - Read back the first cell
  - Read back the second cell
  - Make a drawing of the signals on paper first!
  - Work e.g. in steps of 5 ns
- Add additional capacitance to the bit lines until the circuit stops working

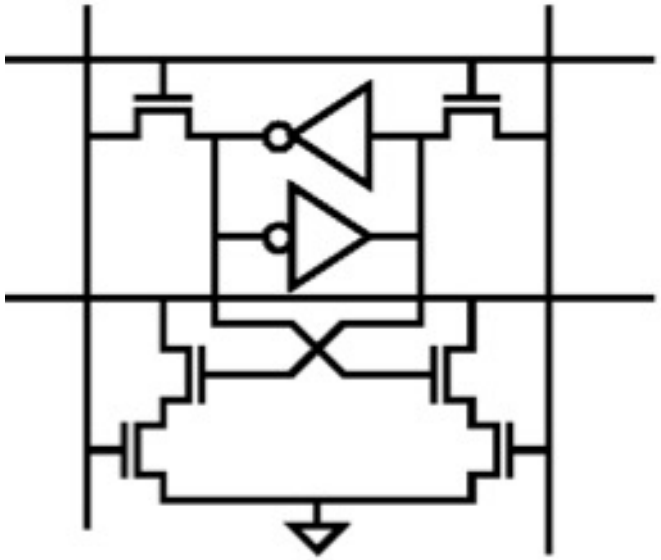
Transistor Dimensions

- Play with the dimensions of the transistors
- Find out in which ranges the cell works

- Check robustness:
  Add an OFFSET of, say, 0.1V to one of the inverters in the SRAM cell (using a VDC source) and repeat the above exercise.

CAM Cell

- Starting from the SRAM cell, make a CAM cell



  - Add a **`match`** signal
  - Use minimal length NMOS with WNMATCH
- Simulate the cell in schematic CAM_SIM:
  - Write 0 as before
  - Precharge the match line
  - Present comparison data at the bit lines (once matching, once mismatching)

Layout – With substrate and NWELL contacts

- In the layout
  - Word and Match shall run horizontally
  - the two bit lines vertically
  - Power can go either way
  - Use only M1 - M3
  - Start with substrate and NWELL contacts *in* the CAM cell

- Before going in layout details, investigate on a paper various options for component and bus placement
  - Make sure cells can be placed directly adjacent to each other (maybe flipped or mirrored)
  - Try to minimize the NWELL area (and spacings) required
  - Keep your findings on 'good' (or 'bad') transistor sizes in mind!

Layout – More compact

The contacts in each cell take quite some space and are not really needed. It is sufficient to contact substrate and NWELL 'here and there'.

If you want:

- Do *not* put substrate or NWELL contacts in each CAM cell.
- Make sure the wells of adjacent cells overlap
- Try to get the cell DRC and LVS clean.
  - You may need to add two more pins…

- Make a row of 8 horizontally abutted cells, and add one substrate and well contact. Make sure you can abut these groups.
- Make a schematic (using bus notation!) and LVS.