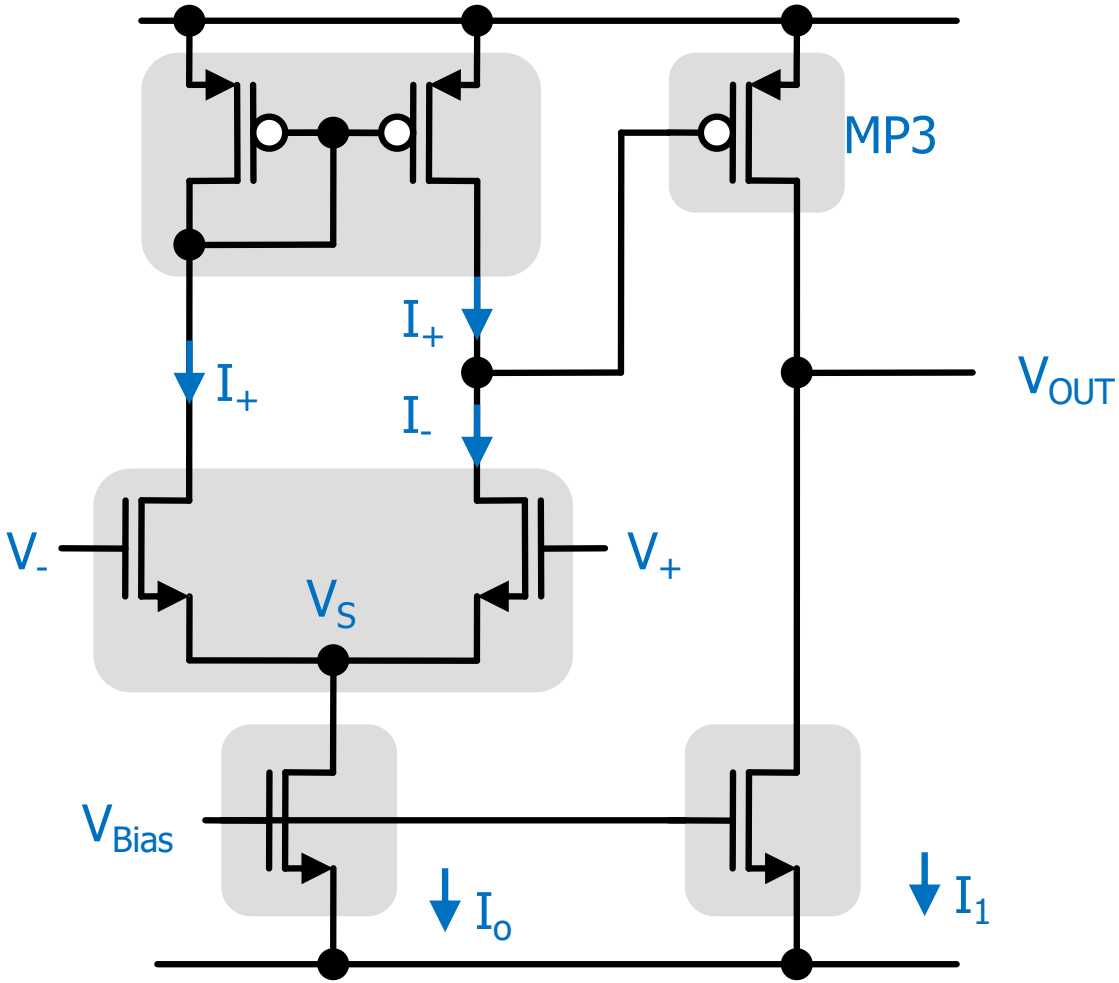
Some More Circuits and Summary

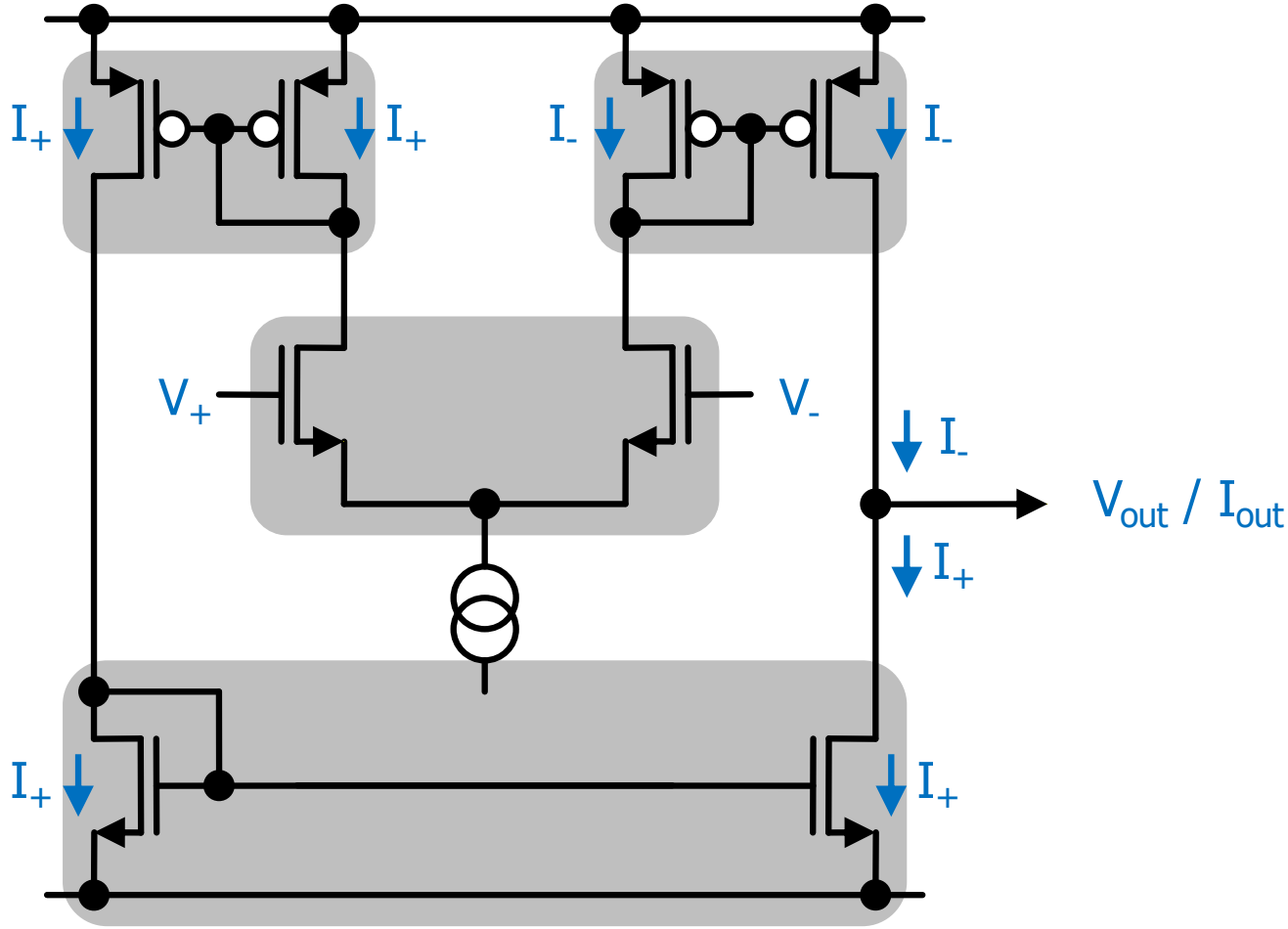
Diff-Amp with Gain Stage



- The differential amplifier is often followed by a gain stage
  - MP3 and I1 are chosen such that the switching points of both amplifiers coincide.
- Advantages:
  - Gains multiply
  - Output dynamic range is increased
- Drawback:
  - Two-stage design has two ‚main' poles and may need compensation if used in feedback configuration.
  - This is an important task in real circuit design!

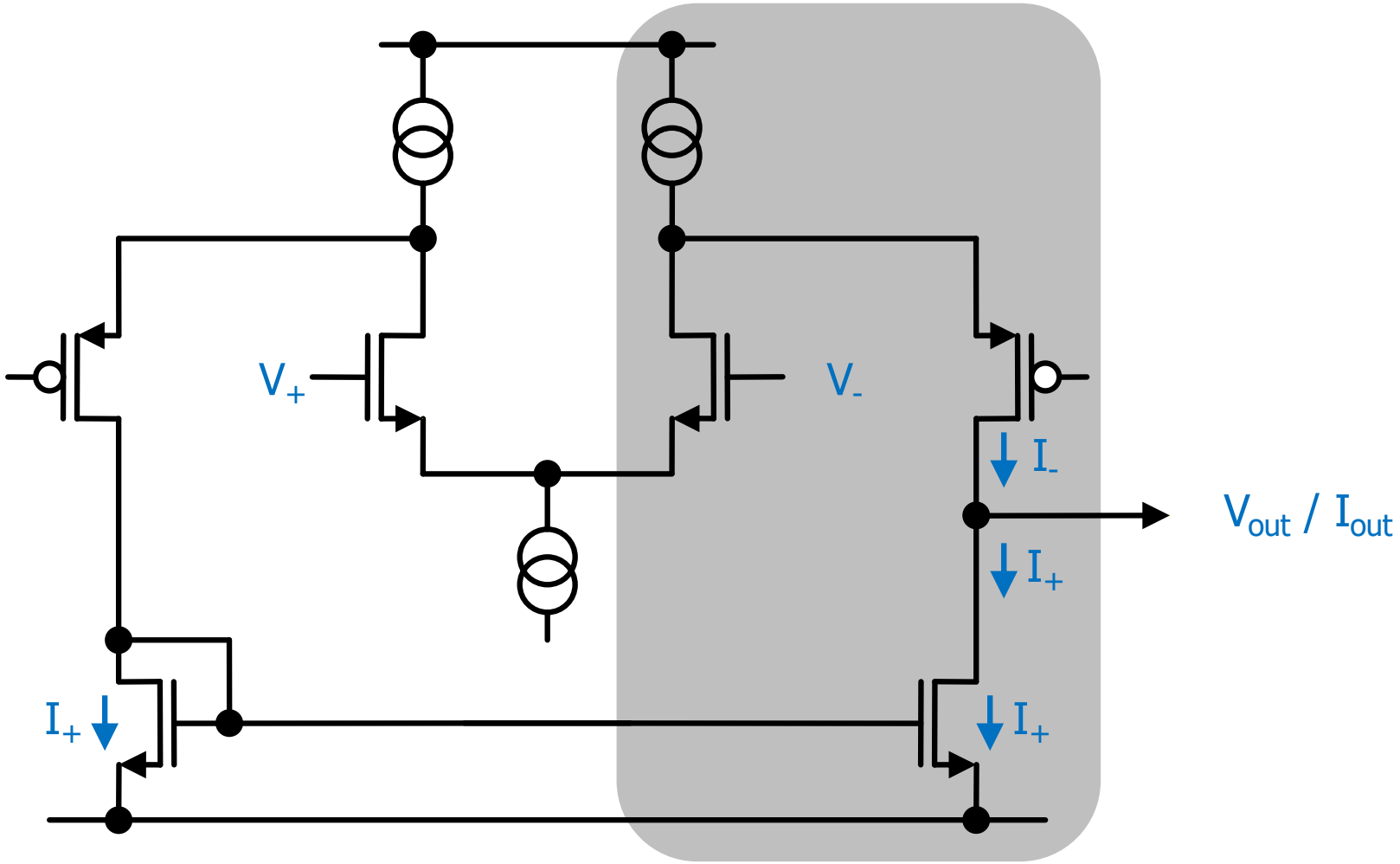
Reminder: Differential Pair + Current Mirror

- The problem of limited output voltage swing for high input common mode can be solved by mirroring the currents:

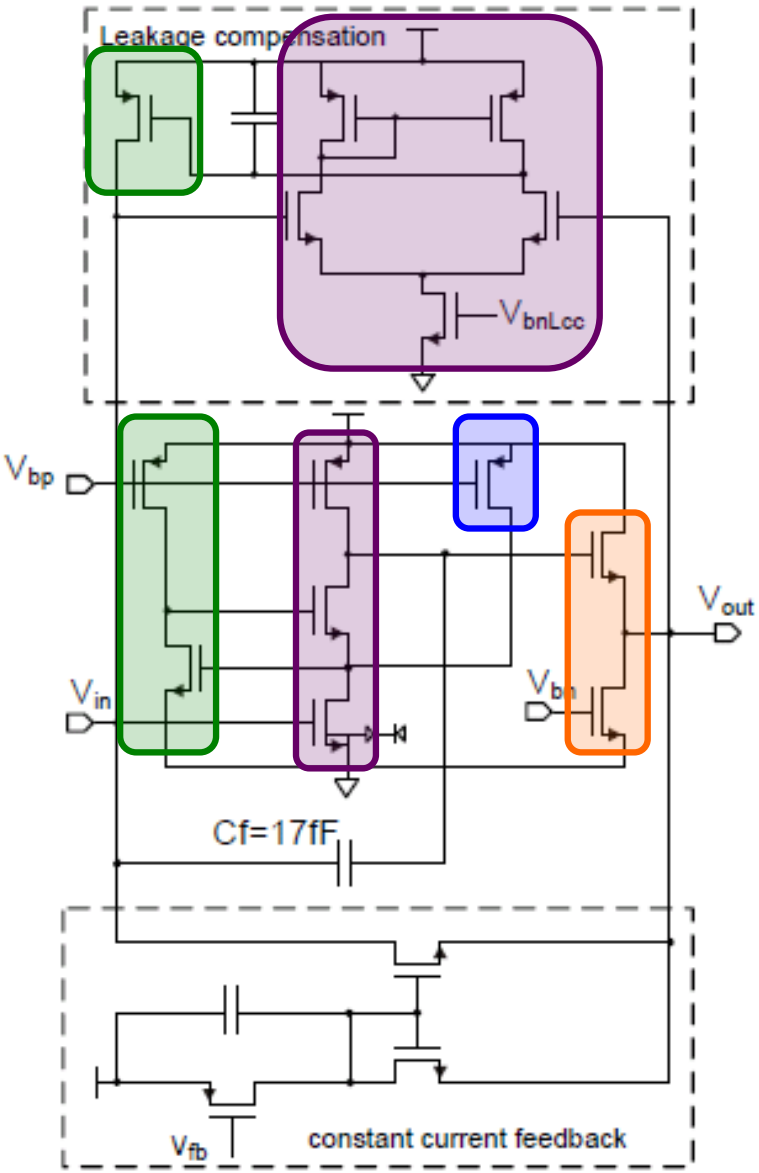


Cascoded differential pair with extra current

- The tricks from the single ended gain stage (added extra current, cascode) can be applied to the diff. pair:



A real ‘charge amplifier’ (ATLAS Pixel)

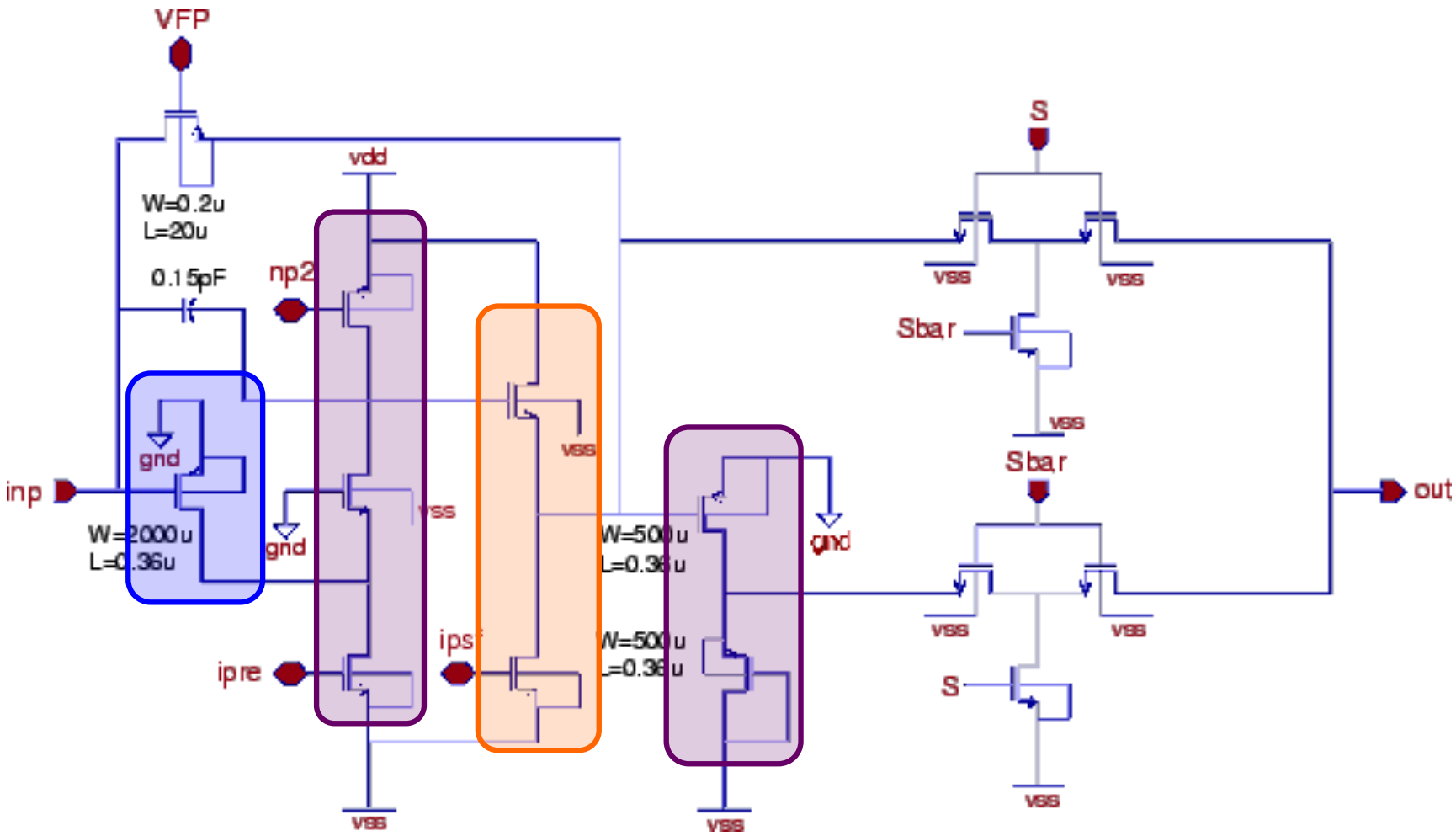


Leakage Compensation:
differential pair
+ current source

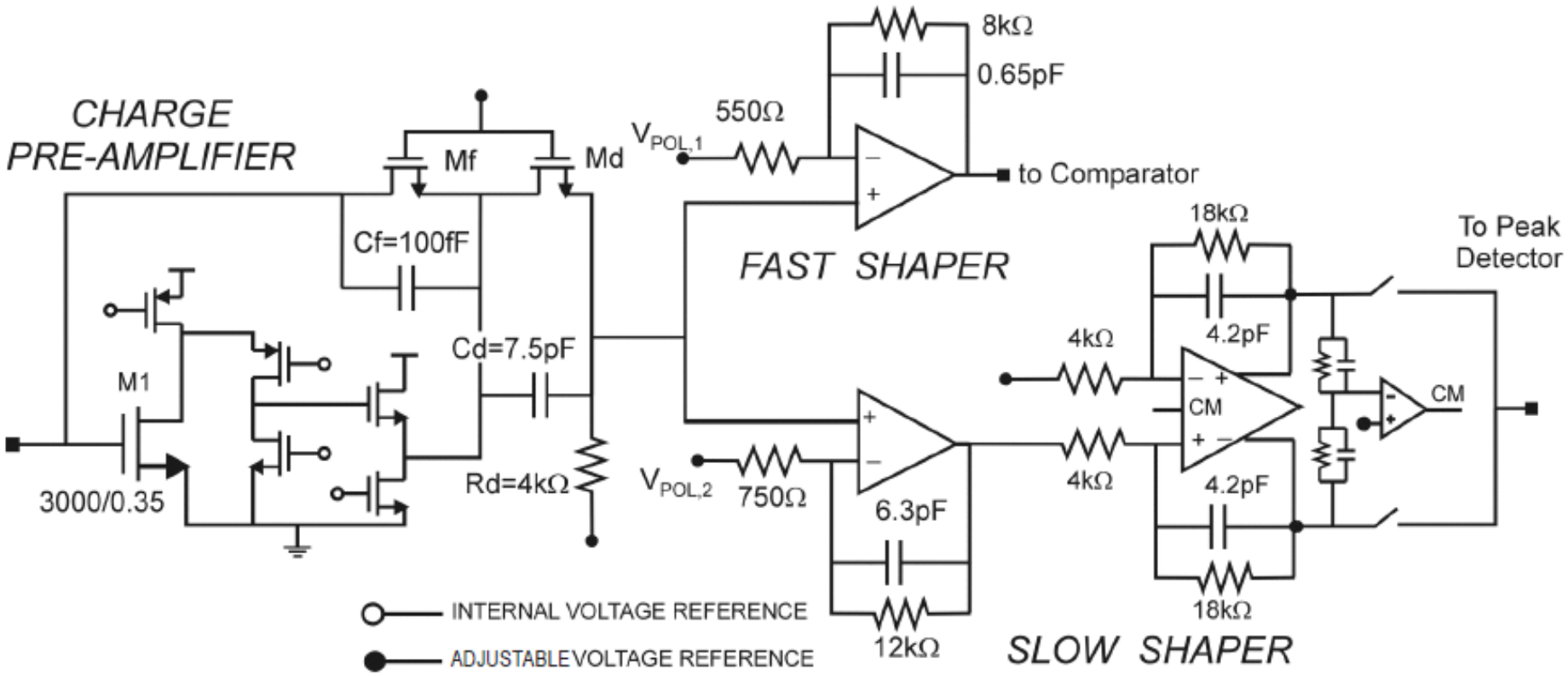
Straight cascode gain stage
+ Regulation
+ Added current
+ Source follower

Constant Current Feedback
(+ ‘magic’ capacitor)

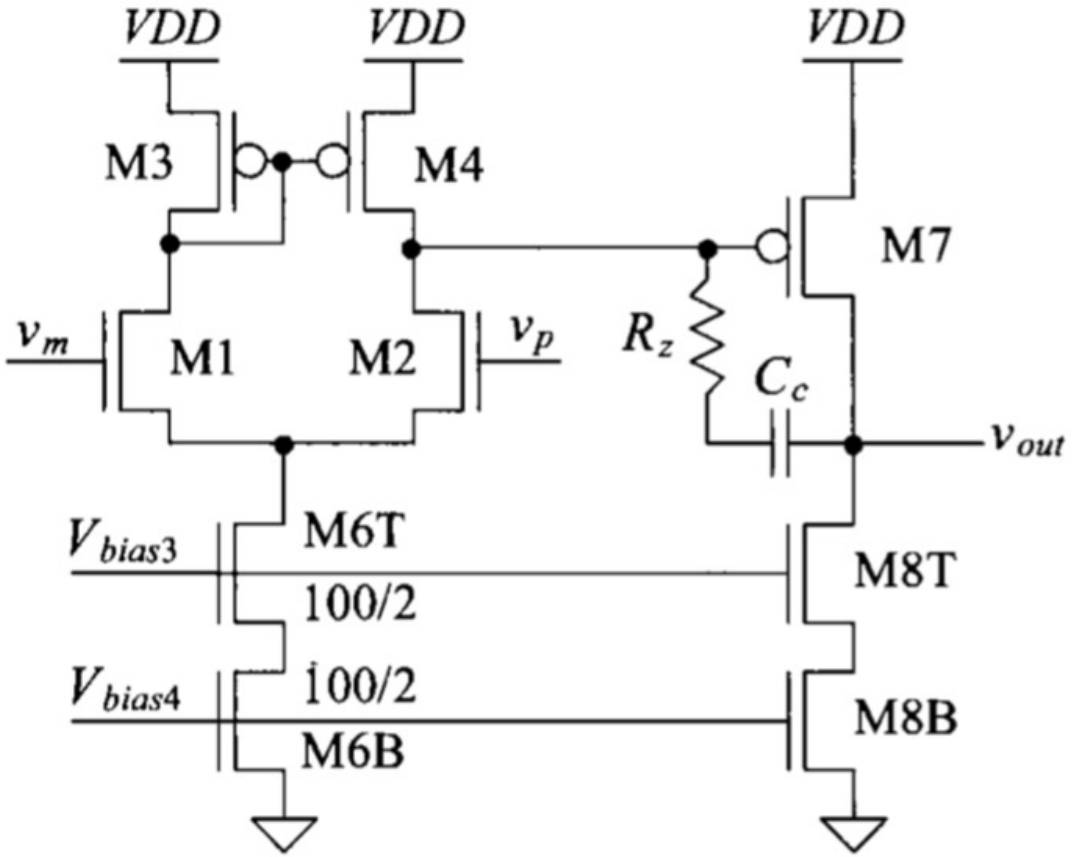
Charge Amplifier 2 ('APV' Chip)

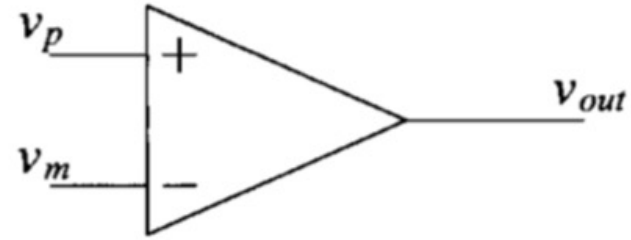


Ladungsverstärker 3 (XYTER)



Simple Operational Transconductance Amp. (OTA)





Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.

From: Wiley: R.J.Baker: CMOS Circuit Design, Layout, Simulation

OTA with (low voltage) Cascodes

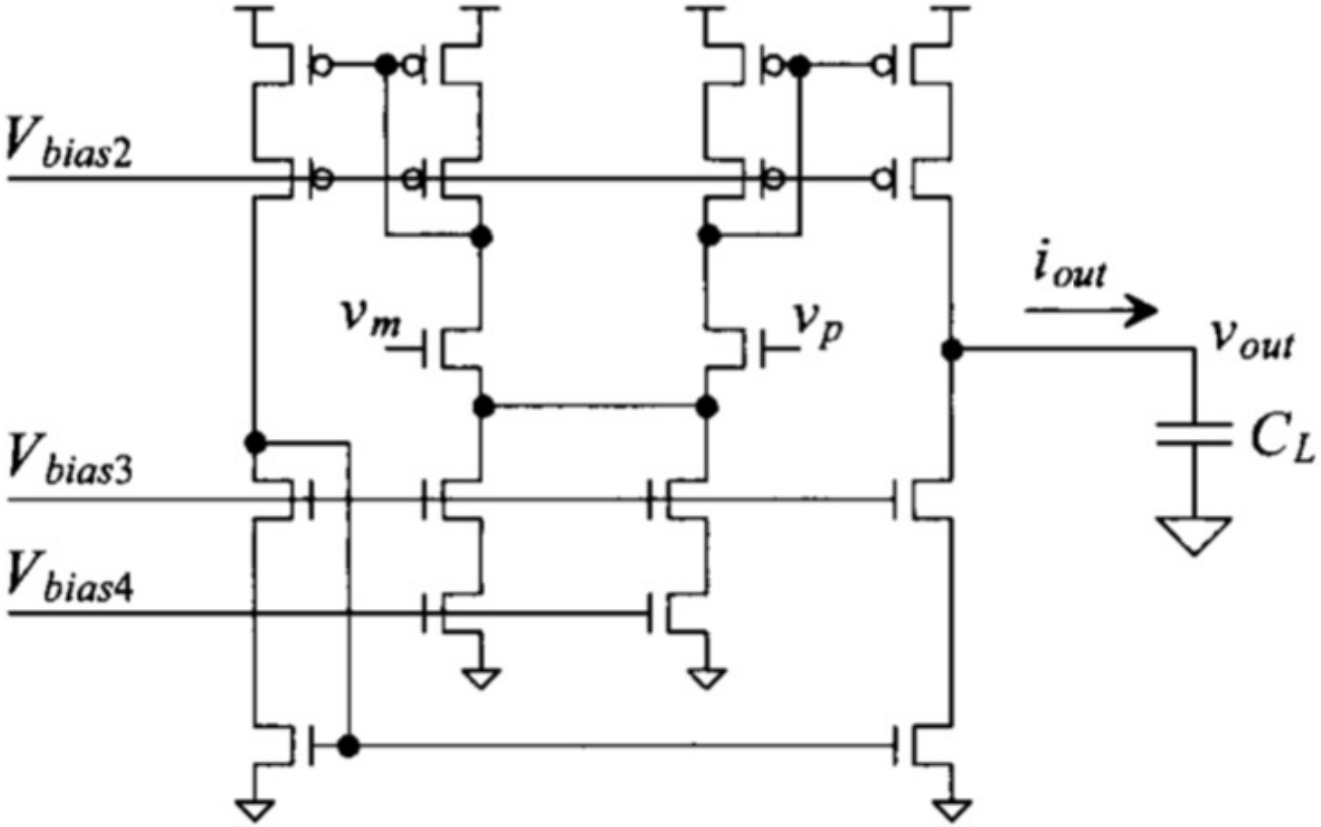
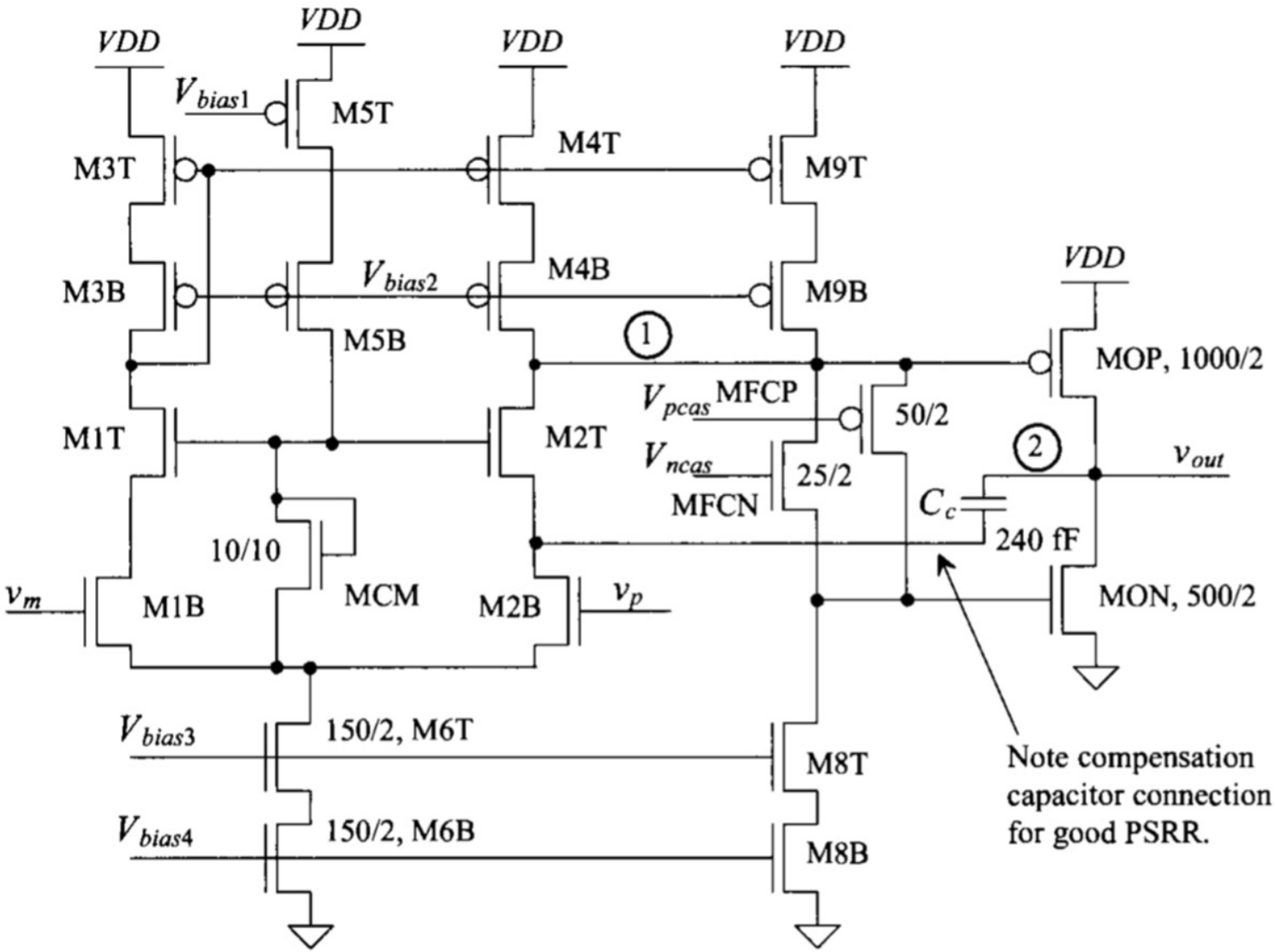


Figure 24.35 A cascode OTA circuit (higher output resistance).

From: Wiley: R.J.Baker: CMOS Circuit Design, Layout, Simulation

CMOS OP-Amp with ('push-pull') buffer



From: Wiley: R.J.Baker: CMOS Circuit Design, Layout, Simulation

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SUMMARY

Summary MOS (1)

- There are NMOS and PMOS transistors
  - They are normally rectangular with channel width W and length L
- The have 4 terminals: G,S,D,B
  - Bulk of NMOS is often connected to global chip substrate and is thus fixed – in particular, it cannot be connected to the source to eliminate substrate effect
- Behaviour is different in
  - strong inversion -> quadratic current law
  - weak inversion -> exponential current law
- For high gate/drain and short devices, there is velocity sat.
- Must distinguish
  - Linear Region (triode / ohmic region): current increases ~ V_{DS}
  - Saturation region: current is rather constant
- Transition between linear / saturation is at $V_{DSat} = V_{GS}-V_{Th}$
  - This depends on gate voltage. Understand why!

Summary MOS (2)

- (Small signal) transconductance
  - 'current gain' = dI_D/dV_{GS}
  - This increases with I_D (s.i.: ~√I, w.i.:~I) and W and 1/L.
- (Small signal) output resistance
  - $r_{ds} = 1/g_{ds}$; $g_{ds} = dI_D/dV_{DS}$
  - This is proportional to I_D and increases with L.
  - High output resistance ('good current source') is good.
- Current can be steered via Bulk (substrate effect)
  - This can be seen as a threshold voltage increase when $V_S > V_B$ (for NMOS)

Summary Circuits

- Most important topologies are
  - Current mirror
  - Gain stage
  - Cascode
  - Source Follower
  - Differential Pair
- Their properties depend on
  - Transistor sizes
  - Currents
  - Bias Points
- Better performance can be achieved by extending the topologies
  - Cascodes
  - Current mirrors
  - ...

Summary Circuits

- Circuits must be brought to the correct operation point
- MOS are mostly operated in saturation
  - To gain dynamic range, operate ‘just at the edge of saturation’
- Small signal models give ‘quick’ insight in the ac behaviour
  - They can be used to understand & optimize circuits
- AC analysis gives more insight in the effect of parameter variations on gain, bandwidth, stability
- Transient Analysis checks the large signal behaviour

Summary Circuits

- (DC) Gain can be modified by tricks
  - increase output resistances with cascodes and/or regulation
  - DC gain of a single MOS (gain stage with ideal current load) is ~20-50 or so.

- Gain-Bandwidth is fundamentally limited by g_m and C_{load}

Exam Topics

- Basic components, parallel, serial connection, Thévenin
- Transfer functions, Bode Plot, Phase shift
- Diode characteristic, capacitance
- MOS in linear and saturated operation, strong/weak inversion, gm, rds, dependence on geometry & current
- Small signal model
- Current mirror, ratio, output conductance, matching. Also with PMOS!
- Cascode in mirror, benefit, biasing, minimum output voltage
- Gain stage (also with PMOS) with different loads, gain, bandwidth, GBW
- Cascoding of gain stage
- Source Follower (NMOS / PMOS)
- Differential pair