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Exercise:
The MOS Transistor

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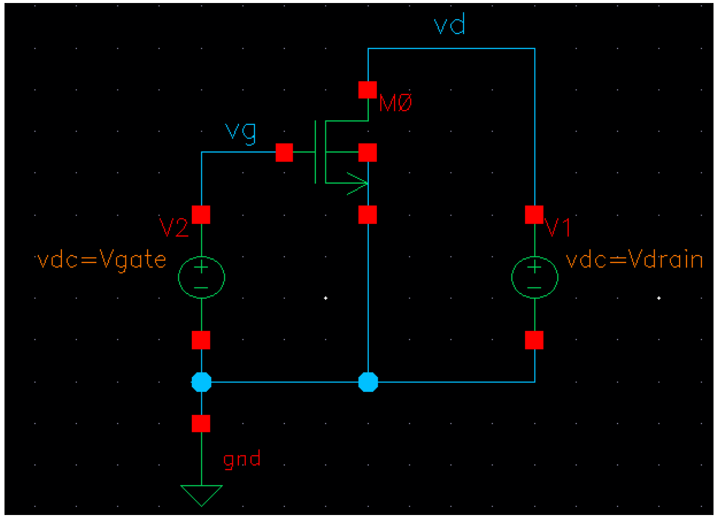
Exercise 1: Simple MOS (Level 1 model)

- We want to simulate a MOS with a very simple model (as the formula shown in the lecture)
- Create a schematic which allows you to set V_G and V_D of a MOS:

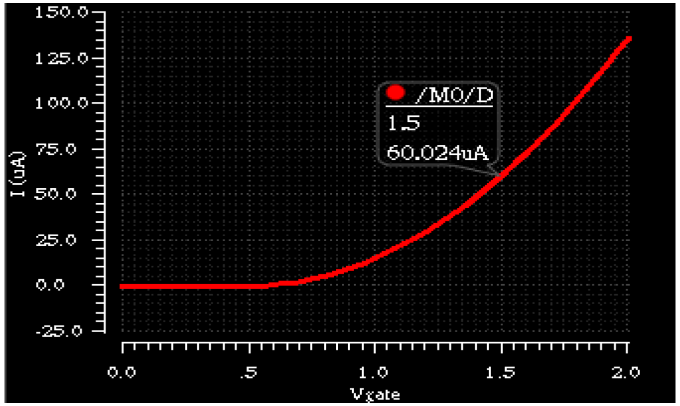


- Use ‘nmos4’ from ‘analogLib’
- Attach the model ‘nmossimple’ (see diode exercise. Add path!)
- Use the following model:

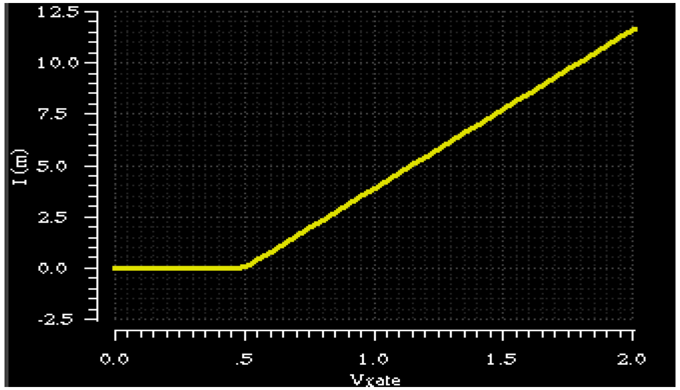
```
.model nmossimple nmos level=1
+ cox=1e-3 kp=100e-6 lambda=0.1 tox=10e-9 gamma=0.5
vto=0.5
```

- Plot
  - I_D for V_G=0..2 V with V_D=2V (Transfer characteristic)
  - $\sqrt{I_D}$ for V_G=0..2 V with V_D=2V (Sqrt of transfer characteristic)
  - I_D for V_D=0..2 V with V_G=1V (Output characteristic)

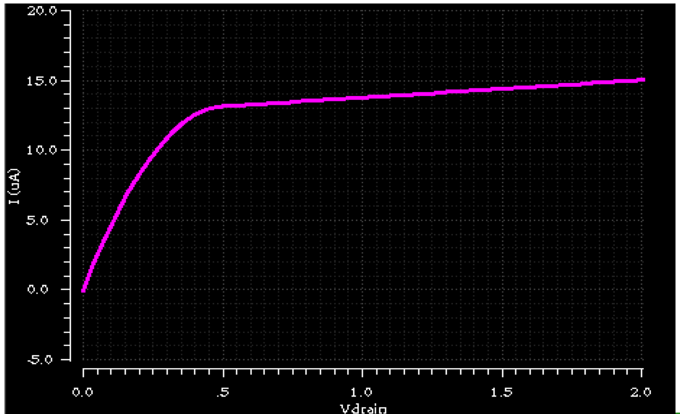
Solution 1



- Transfer (linear y scale)
  - Current at V_G=1.5V is
    $I_D = K/2\ (V_G - V_T)^2 (1 + \lambda\ V_D)$
    $= 50 \times 1 \times (1 + 0.1 \times 2)\ \mu A$
    $= 50 \times 1.2\ \mu A = 60\ \mu A$



- Sqrt(..) plot shows exact quadratic behaviour (‘level 1 model’)



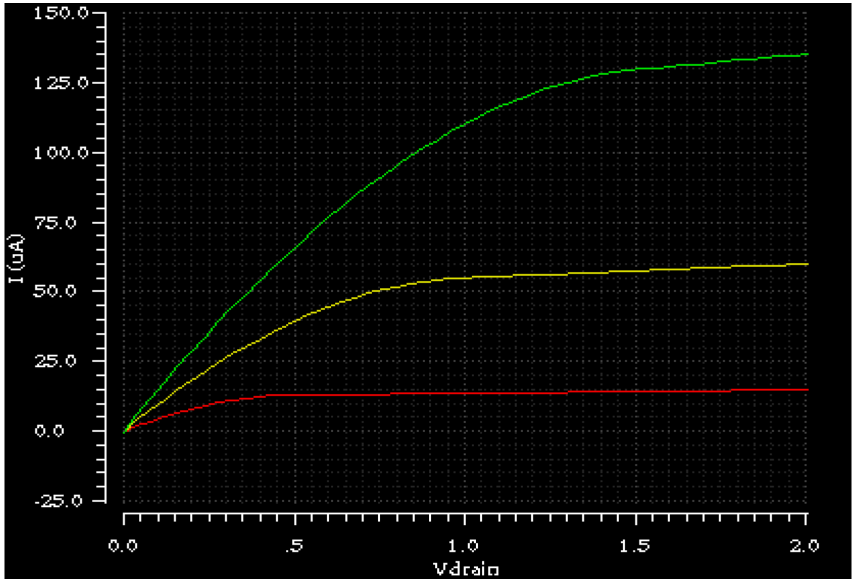
- Output Char. shows Early effect
  - Current at kink is
    $I_D = K/2\ (V_G - V_T)^2 (1 + \lambda\ V_D)$
    $= 50 \times 0.5^2 \times (1 + 0.1 \times 0.5)\ \mu A$
    $= 12.5 \times (1.05)\ \mu A$

Exercise 2: Output Resistance

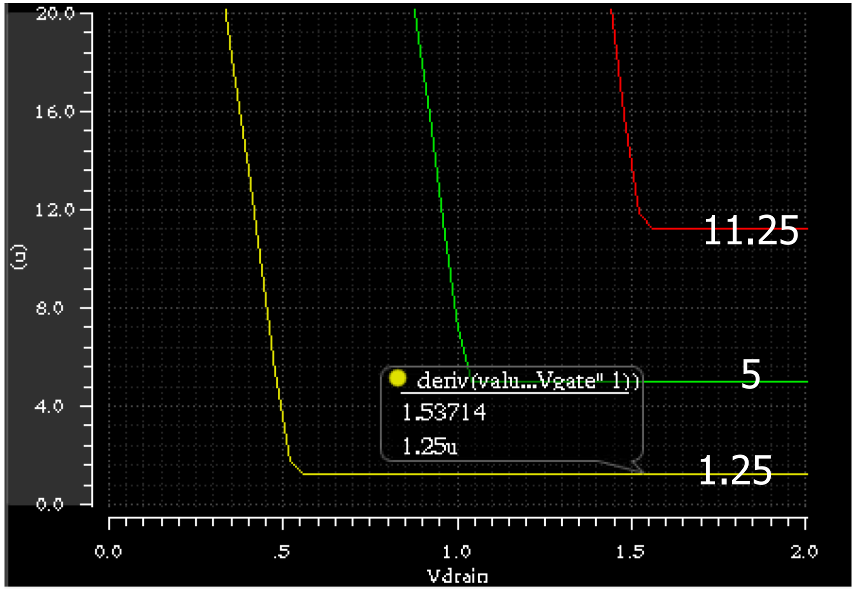
- Sweep I_D for V_D=0..2 V with V_G=1V, 1.5V, 2V

- What are the slopes at high drain voltages ?
- Do they correspond to what you expect ?

Solution 2



- Saturation point increases
- Current increases

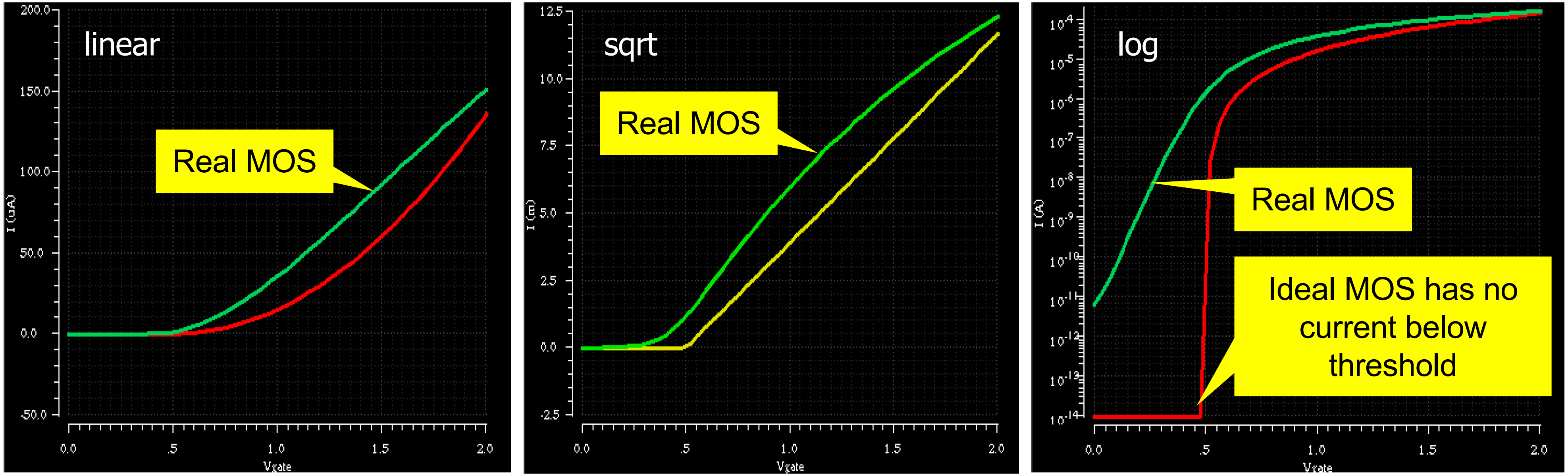


- $I_D = K/2\ (V_G - V_T)^2(1 + \lambda\ V_D)$
- $dI_D/dV_D = \lambda\ K/2\ (V_G - V_T)^2$
  $= 0.1 \times 50 \times (0.5/1/1.5)^2$
  $= 5 \times (0.25/1/2.25)$
  $= 1.25/5/11.25$ S
  as simulated!

Exercise 3: A real MOS

- Now use the model 'nmos' provided in the file **`MOSLib.lib`** on the course web site (this MOS should be operated below 2V)
- Compare the transfer curves of a 'nmossimple' and 'nmos'
  - Are they both exactly quadratic?
  - What happens at low gate voltages (below threshold)?
    Do a logarithmic plot!

Solution 3:



- Real MOS is not quadratic
  - Velocity saturation at high Gate voltages
  - Current >0 in weak inversion (below threshold)

Exercise 4: Sizing the MOS

- Set the properties W and L of both types of MOS to WL
- Compare the output characteristics for W,L=1u and W,L=10u for both MOS
  - Is there a change in output resistance if you change the geometry?

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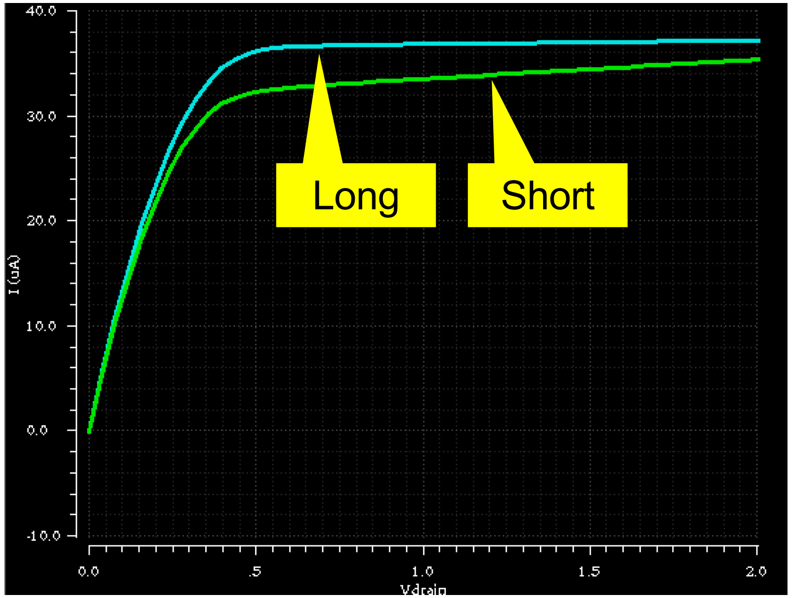
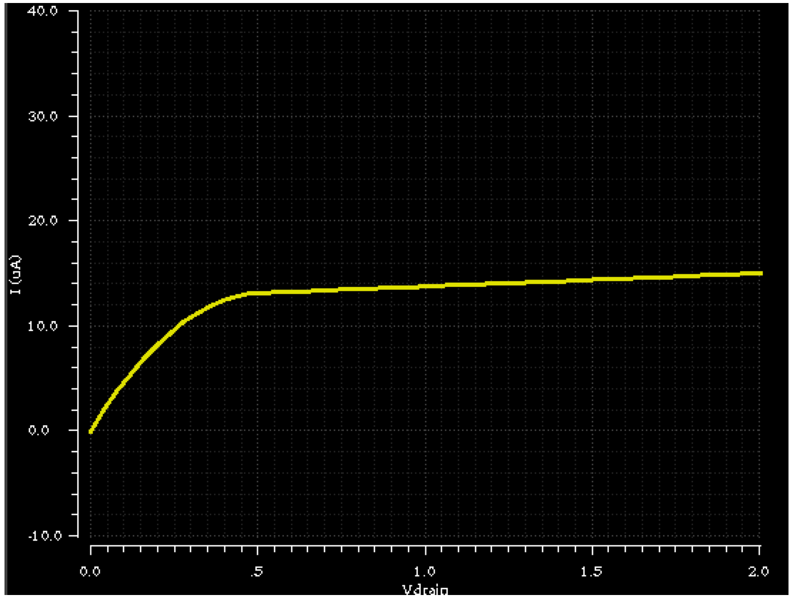
Solution 4:



- For the real MOS, the output resistance increases, when L is increased



- For the ‘nmossimple’ , there is NO difference (both curves are the same). This model is clearly too simplistic!

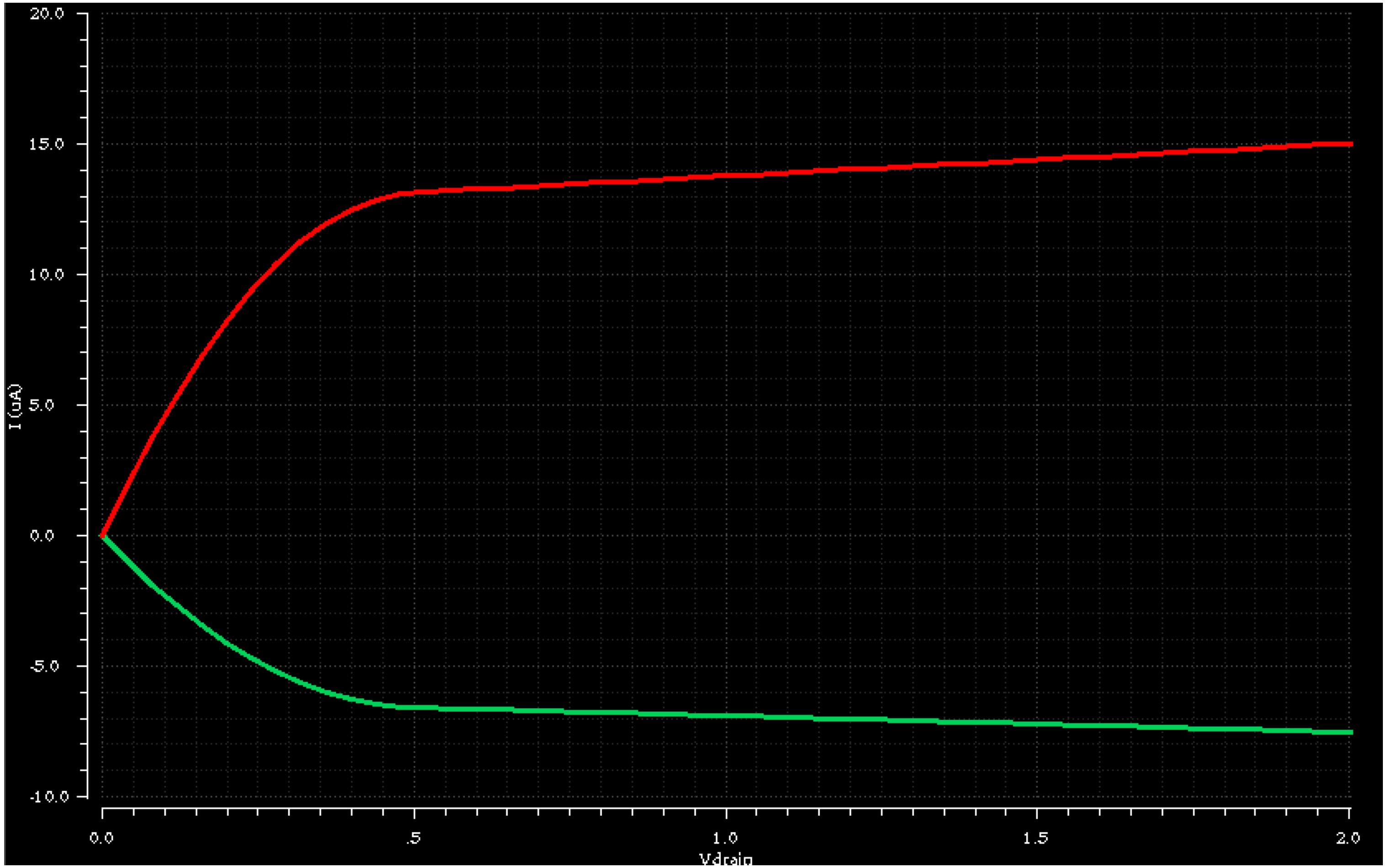
Exercise 5: PMOS

- Simulate transfer and output characteristic for a PMOS
  - Note that the source of the transistor is now ‚on top'
  - Gate and drain must be negative with respect to source

- Simulate in parallel a NMOS of the same size.
  - Plot the drain current of NMOS and PMOS simultaneously.
  - How big is the difference?
  - Does that fit the model?

Solution 5

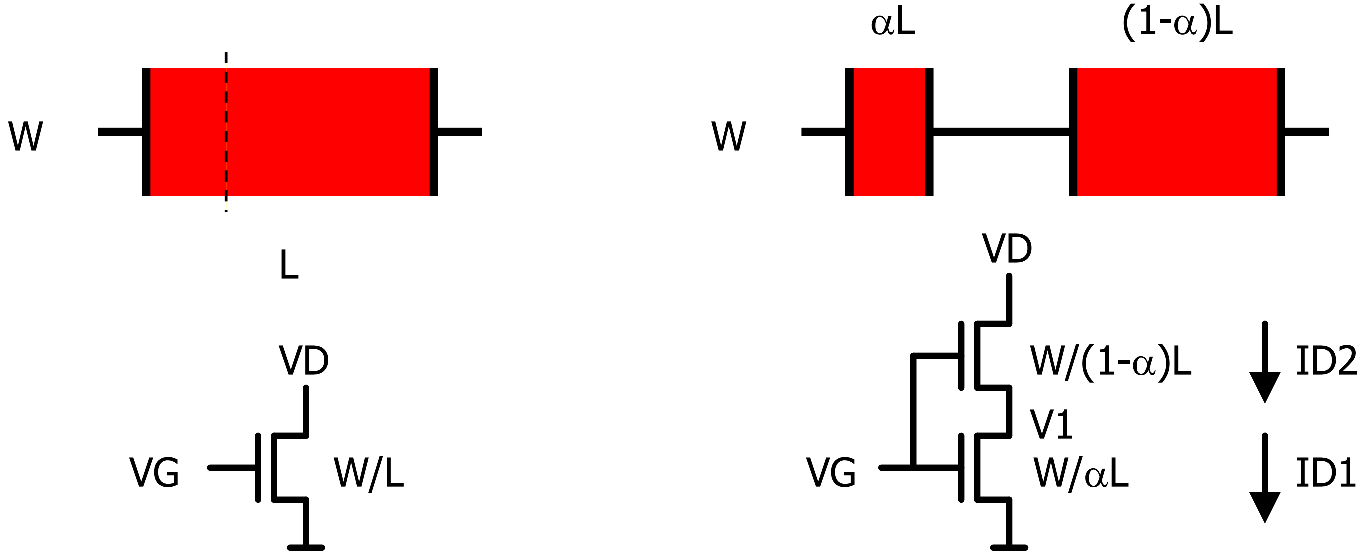
- Here for simple models:



- Ratio is exactly 3, the ratio of the kp parameters

Exercise 6: Do Formulae match ?

- A MOS with width W and length L is cut in two devices with lengths αL and (1-α)L:



- The series connection must behave as the single device!
- Assume a large VD. In which regimes do the 2 MOS operate (lin. / sat.?). Write down the formulae for ID1 and ID2
- The currents must be equal. Find α. Then find ID1 (=ID2)
- Is this the current of the single MOS?
- How large is V1 for α=5/9 ?

Solution 6:

```
In[63]:= ILin[Vgs_, Vds_] = (Vgs - Vt) Vds - 1/2 Vds^2;
         ISat[Vgs_, Vds_] = 1/2 (Vgs - Vt)^2;
```

- These expressions do not yet contain W/L
- We set K=1 for simplicity

```
In[91]:= EQ1 = W/(α L) ILin[VG, V1] == W/((1 - α) L) ISat[VG - V1, VD - V1] // Simplify
```

$$\text{Out[91]=}\quad \frac{W\left(V1^2 - 2\,V1\,(VG - Vt) + (VG - Vt)^2\,\alpha\right)}{L\,(-1+\alpha)\,\alpha} == 0$$

- Lower MOS is in linear region, drain voltage is V1
- Upper MOS is in saturation. Vgs and Vds are relative to VS, in this case V1!

```
In[67]:= αsol = α /. First@Solve[EQ1, α] (* find α *)
```

$$\text{Out[67]=}\quad \frac{-V1^2 + 2\,V1\,VG - 2\,V1\,Vt}{(VG - Vt)^2}$$

(find α for a *given* V1!)

```
In[69]:= I2 = W/(α L) ILin[VG, V1] /. α -> αsol // Simplify (* Find current *)
```

$$\text{Out[69]=}\quad \frac{(VG - Vt)^2\,W}{2\,L}$$

```
In[71]:= I2 == W/L ISat[VG, VD] // Simplify (* Compare to single MOS *)
Out[71]= True
```

Great: everything is consistent

```
In[72]:= $Assumptions = VG > Vt;
In[73]:= V1sol = V1 /. First@Solve[EQ1, V1] // Simplify
```

$$\text{Out[73]=}\quad -(VG - Vt)\left(-1 + \sqrt{1-\alpha}\right)$$

```
In[74]:= V1sol /. α → 5/9
```

$$\text{Out[74]=}\quad \frac{VG - Vt}{3}$$

Solution 6 – remark:

- This is also consistent, if both are in linear region:

Both in linear regime:

In[12]:= $\texttt{EQ1} = \frac{W}{\alpha\, L}\,\texttt{ILin[VG, V1]} == \frac{W}{(1-\alpha)\, L}\,\texttt{ILin[VG - V1, VD - V1] // FullSimplify}$

Out[12]= $\frac{V1\ (V1 - 2\, VG + 2\, Vt)\ W - VD\ (VD - 2\, VG + 2\, Vt)\ W\, \alpha}{L\ (-1 + \alpha)\ \alpha} == 0$

In[13]:= `αsol = α /. First@Solve[EQ1, α] (* find α *)`

Out[13]= $-\frac{V1\ (V1 - 2\, VG + 2\, Vt)}{VD\ (-VD + 2\, VG - 2\, Vt)}$

In[14]:= $\texttt{I2} = \frac{W}{\alpha\, L}\,\texttt{ILin[VG, V1] /. α → αsol // Simplify (* Find current *)}$

Out[14]= $-\frac{VD\ (VD - 2\, VG + 2\, Vt)\ W}{2\, L}$

In[15]:= $\texttt{I2} == \frac{W}{L}\,\texttt{ILin[VG, VD] // Simplify (* Compare to single MOS *)}$

Out[15]= True