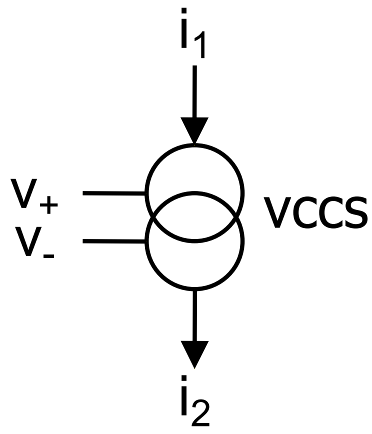
RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

Exercise:
Abstract Circuits

Prof. Dr. P. Fischer

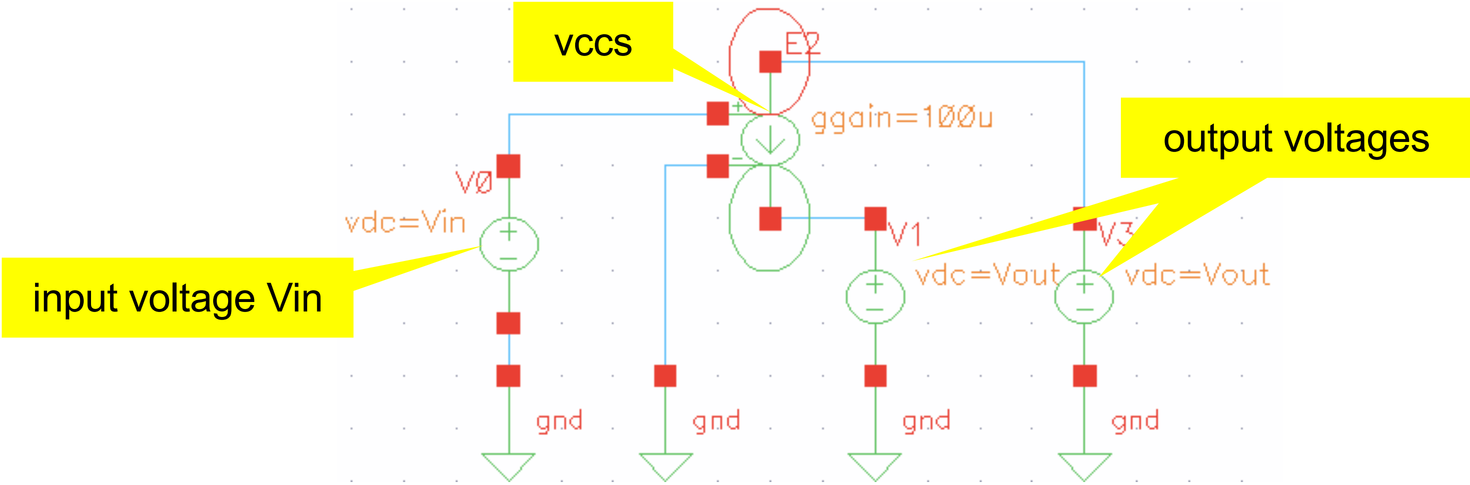
Lehrstuhl für Schaltungstechnik und Simulation
Uni Heidelberg

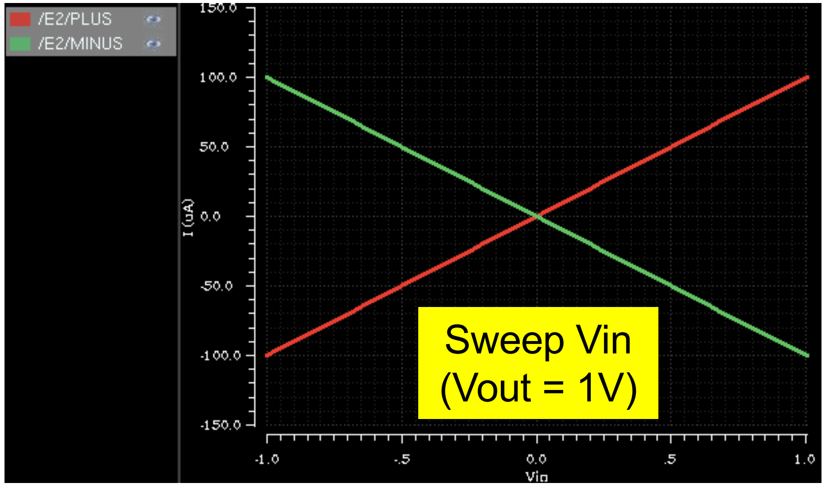
Exercise 1: voltage controlled current source

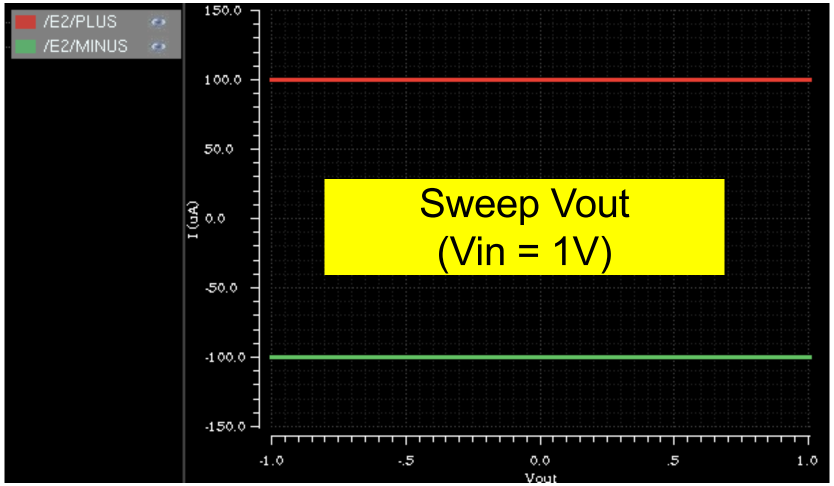


- The drain current in a transistor depends on the gate voltage. It can therefore be considered as a **v**oltage **c**ontrolled **c**urrent **s**ource 'vccs'
- In the analogLib, the vccs has a differential input and two outputs of opposite signs: $i_1 = G\,(v_+ - v_-)$, $i_2 = -\,i_1$
- Set up the following circuit
  - Use a vccs with gain = 100 µS
  - Connect v_- to ground and v_+ to a dc voltage V_{IN}
  - Connect the i_1 and i_2 outputs to V_{OUT1} = 1V and V_{OUT2} = 1V
- Now
  - Sweep VIN (DC sweep, for instance from -1V to 1V) and observe the currents in the output voltage sources. Change the gain of the vccs and observe the effect.
  - Does the output **current** for a given V_{IN} depend on the V_{OUT} ?

Solution 1

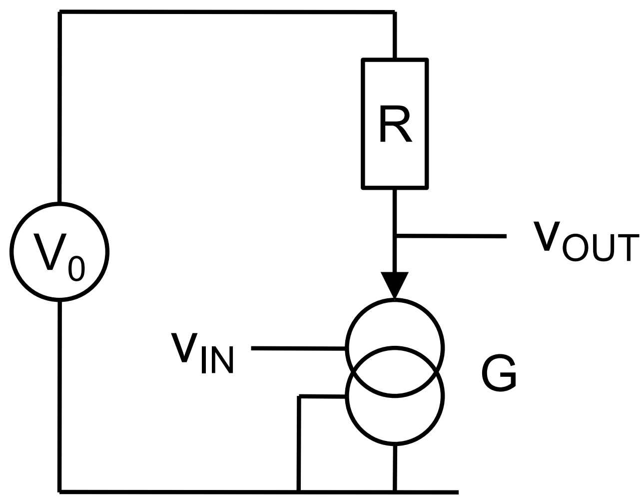






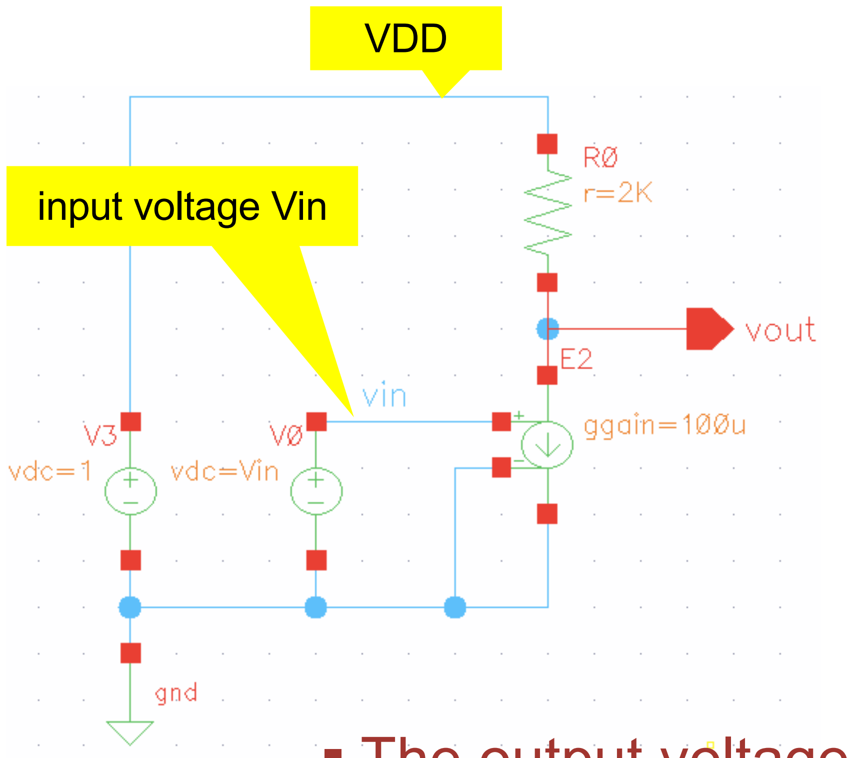
- The output current of these *ideal* sources does not depend on the output voltage

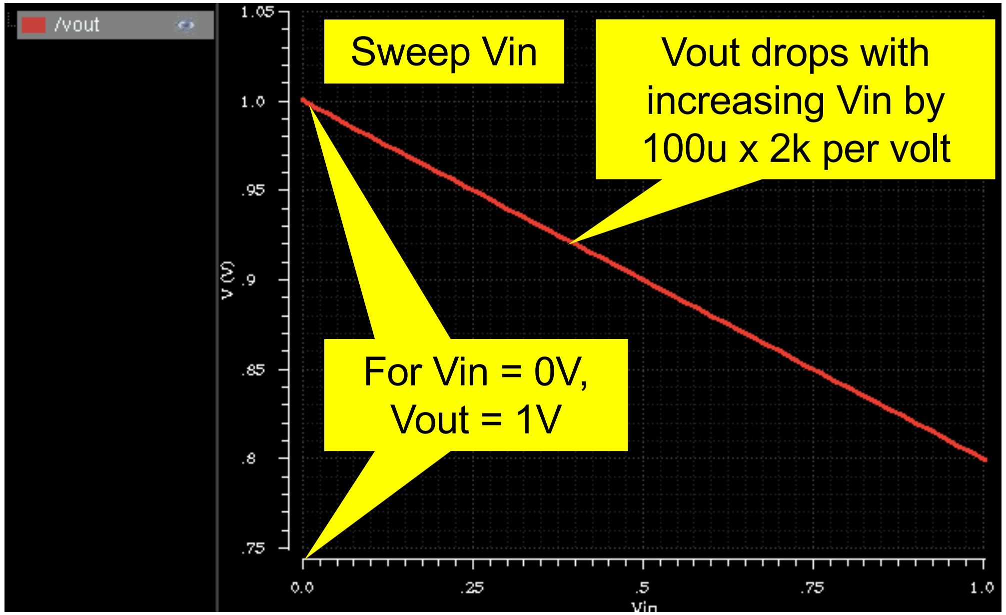
Exercise 2: Idealized Amplifier 1



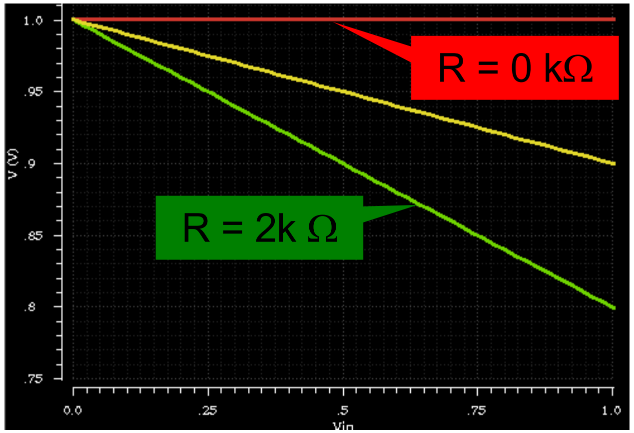
- Implement the following circuit:
  - The current from the vccs is sent to a resistor R
- Start with
  - G = 100 µS
  - R = 2 kΩ
  - V_0 = 1 V
- Simulate:
  - How does v_{OUT} change when v_{IN} changes (e.g. from 0 to 1 V) ?
  - Explain (Calculate) ! Write down the current equation at node v_{out} and use $i_{VCCS} = G\, v_{in}$
  - What is the gain of the circuit dV_{OUT} / dV_{IN}?
  - Change R and G in your simulation. Is the effect as expected (as calculated)?

Solution 2





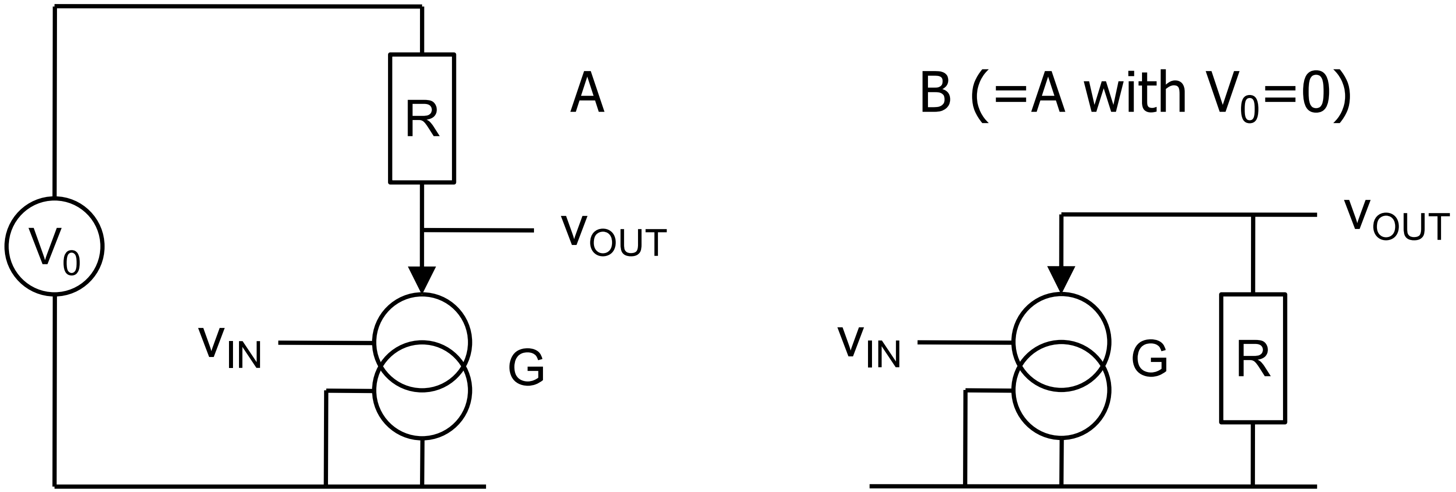
- The output voltage is $V_{out} = VDD - R \times I = VDD - R\, G\, V_{in}$
- The gain (slope) is $v = dV_{out} / dV_{in} = - R\, G$
- Changing R (0, 1kΩ, 2kΩ):



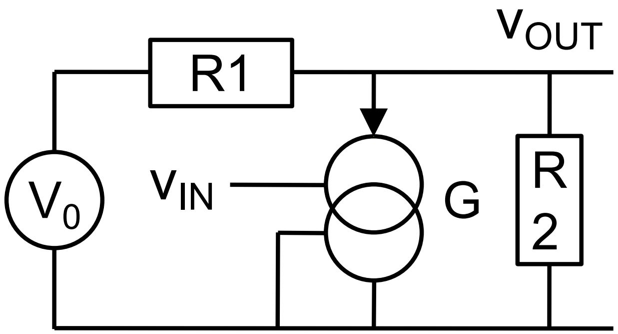
RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

Exercise 3: Idealized Amplifier 2

- In the previous circuit, change V_0. What happens with the *DC offset* of the output and with the *gain*? Explain!
- So, what is the difference between the following two circuits A,B ?

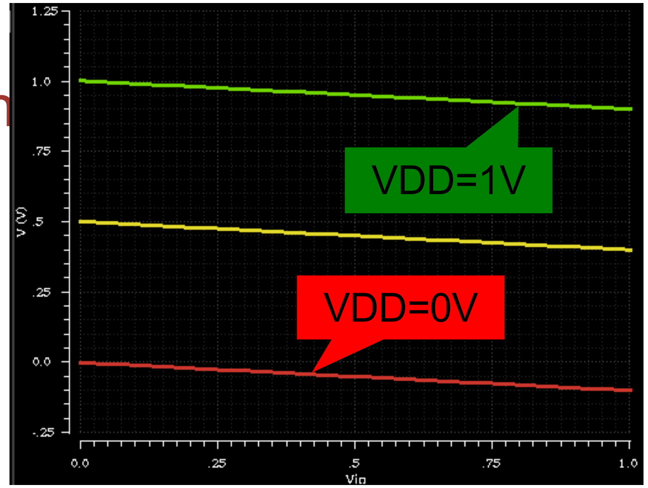


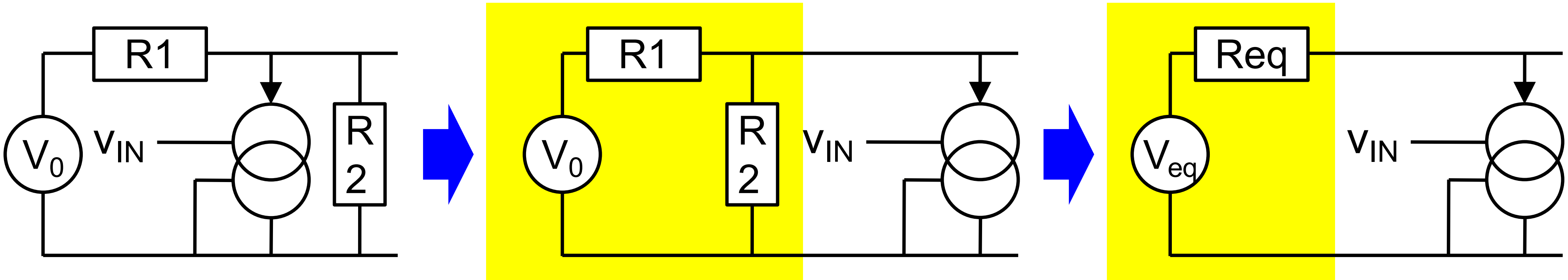
- **PREDICT** the gain ($V_{IN} \rightarrow V_{OUT}$) of the following circuit (Thénevin!):
- Verify this by simulation (for instance R1 = 1 kΩ, R2 = 2 kΩ)
- What happens when you exchange R1 and R2?



Solution 3

- Changing VDD just changes the off-set (i.e. shifts the curve up and down
  - With the ideal source, the circuit also works at VDD=0V.
- The gain of the two circuit is the same. For a gain analysis, we can drop VDD for simplicity!



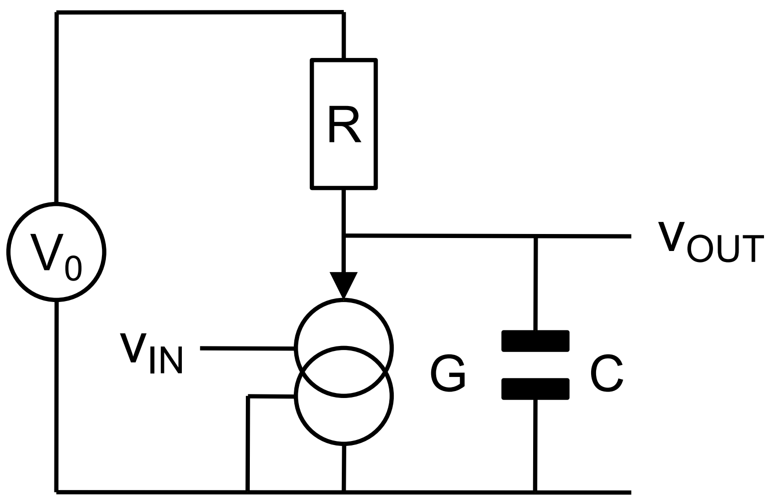


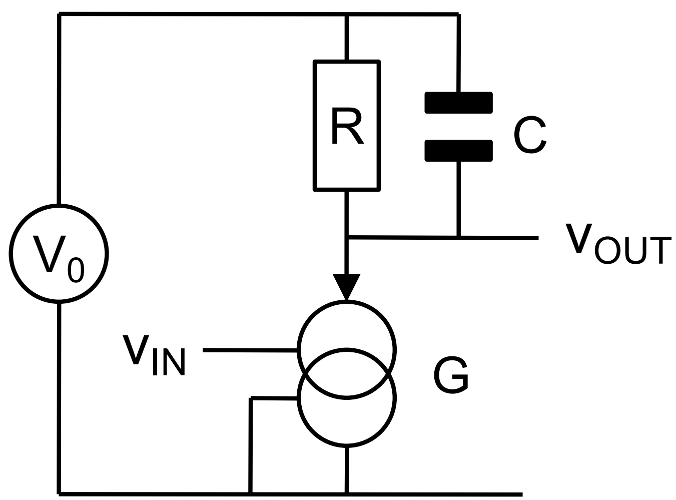
- $V_0/R_1/R_2$ can be replaced by V_{eq}/R_{eq}. R_{eq} is $R_1 \parallel R_2$. V_{eq} is irrelevant for gain. Gain becomes G R_{eq}.
- Gain is -100uA × 2kΩ / 3 = - 0.066.
- Swapping R_1/R_2 makes no difference!

RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

Exercise 4: Idealized Amplifier 3

- Load the output with a capacitor (1 pF) to ground (left) and make an *ac* sweep. What is the dc gain?
- Where is the corner frequency? Why?

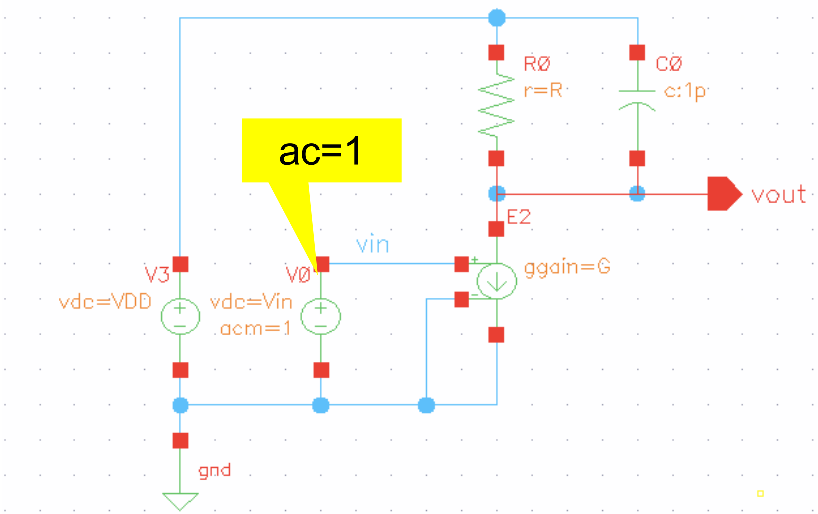


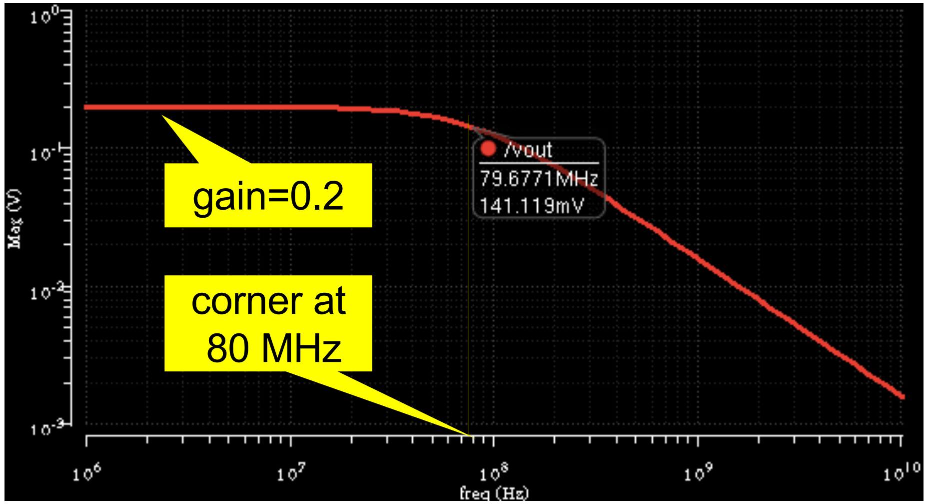


- Now try the right circuit. Is there a difference? Explain!
- Draw an equivalent circuit without V_0!

Solution 4

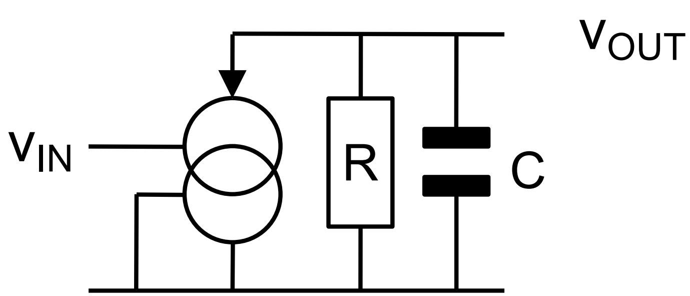
- Remember to add an ac component to V_{in}!





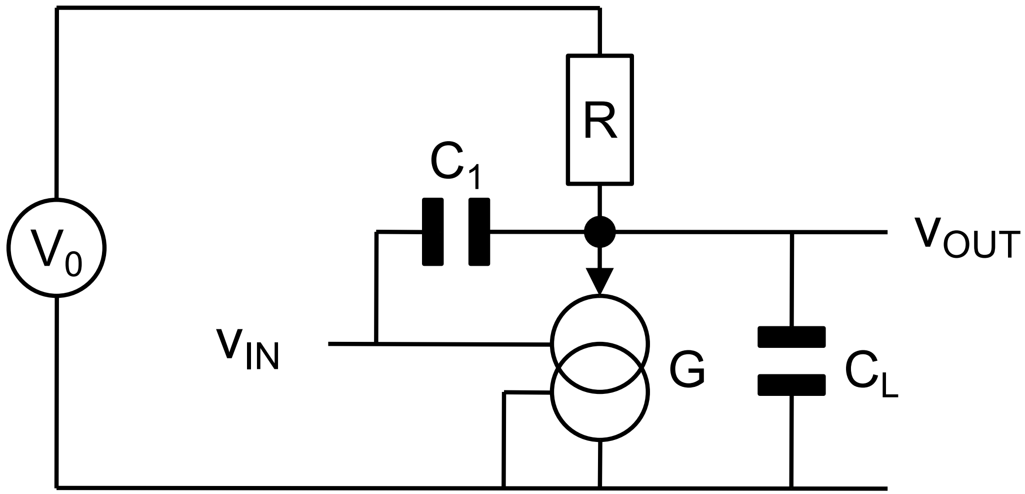
- We see a Low Pass behavior
  - DC gain is 100u x 2k = 0.2
  - Corner is at ω=1/RC=1/2n=500M $\rightarrow$ ν = 500M/6.28 = 79.6 MHz
- Derivation by current sum at v_{out}:
  - $G\, v_{in} + v_{out}/R + v_{out}\, s\, C = 0$

$$\rightarrow v_{out} / v_{in} = -\frac{G\,R}{1 + C\,R\,s}$$



Exercise 5 (advanced!): More capacitors

- Consider this circuit with an extra C_1 between V_{IN} and V_{OUT}



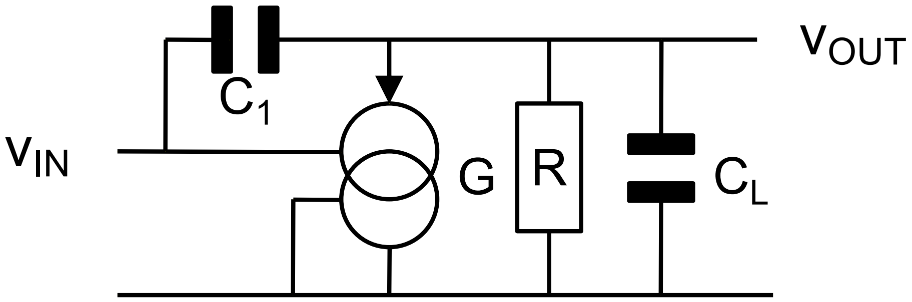
- Draw the circuit without V_0!
- What gain do you expect at *dc* ? Sign?
- What gain do you expect for *very* high frequencies? Sign?
- Calculate the transfer function H[s] and the gain
  - Verify your predictions
- Simulate the circuit

Exercise 5 cont. (For fun)

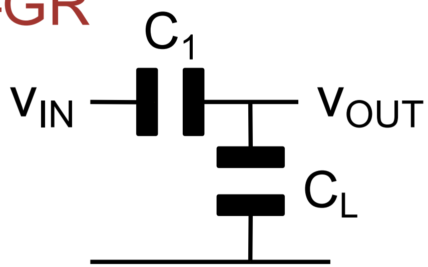
- Where is the pole, where is the zero?
- Chose the resistor value such that the pole and the zero are at the same frequency.
  - Does that always work?
  - What is the DC gain?
  - How does the transfer function look like?
  - What is the gain of the circuit vs. frequency?

Solution 5

- All elements to VDD to to ground:



- Gain at DC (no caps) should be as before –GR
- At high frequencies, impedances of C dominate. We have a capacitive divider with gain + $C_1/(C_1+C_L)$ (positive!)



- Derivation (current sum at v_{out}):

```
Solve[(vout - vin) s C1 + G vin + vout/R + vout s C == 0, vout]
```

$$v = -G\,R\,\frac{1 - \frac{C1}{G}\,s}{1 + R\,(CL + C1)\,s}$$

```
v /. s → 0
```

$$-G\,R$$

```
Limit[v, s → ∞]
```

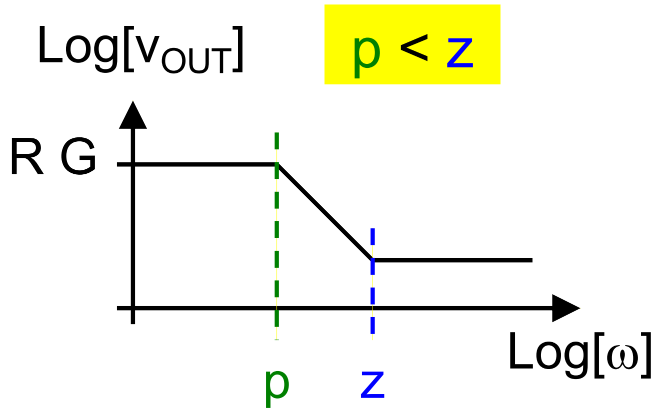
$$\frac{C1}{C1 + CL}$$

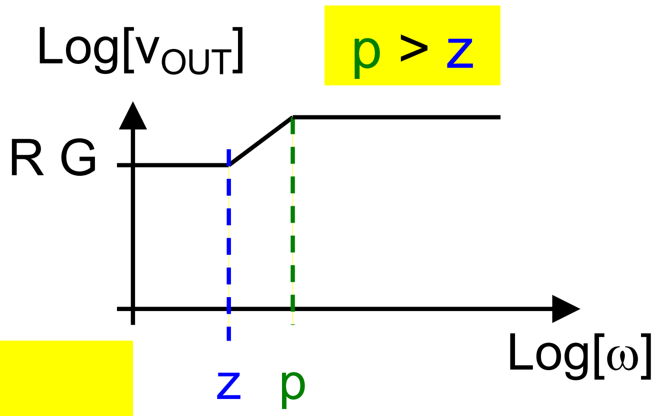
© P. Fischer, ZITI, Uni Heidelberg

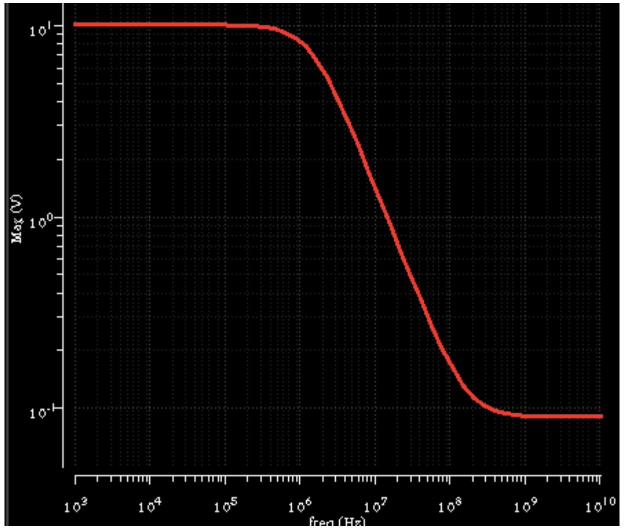
Solution5

$$v = -R\,G\,\frac{1 - C1\,/\,G\,s}{1 + R\,(CL + C1)\,s}$$

- We have a pole at $p=1/R(C_1+C_L)$ and a ZERO at $z=G/C_1$
- Gain changes from negative to positive!
- Bode Plot depends on weather pole or zero is higher frequency







Example for $p > z$:
$G=100u$, $R=100k$, $C_1=0.1p$, $C_L=1p$
$p = 1/R(C_1+C_L) \sim 1/RC_L = 10MHz$
$z = G/C_1 = 1GHz$

Solution 5

- Setting pole and zero equal is always (i.e. for all values of C1, CL, G) possible:

```
In[48]:= Solve[z == p, R]
```

Out[48]= $\left\{\left\{R \to \frac{C1}{(C1 + CL)\ G}\right\}\right\}$

- (Note: This is not the case for, e.g., CL, which may have to be negative..)

```
In[40]:= Solve[z == p, CL] // Simplify
```

Out[40]= $\left\{\left\{CL \to C1\left(-1 + \frac{1}{G\ R}\right)\right\}\right\}$

- The DC gain is –C1/(C1+CL):

```
In[49]:= v /. R → Requal /. s → 0 // Simplify
```

Out[49]= $-\frac{C1}{C1 + CL}$

- The transfer function is just

$$-\frac{C1}{C1 + CL}\ \frac{G - C1\ s}{G + C1\ s}$$

Solution 5

- The s-part of this function has the form (1-ks)/(1+ks).
- With s = i ω, the absolute value is calculated by multiplying with the complex conjugate, i.e.

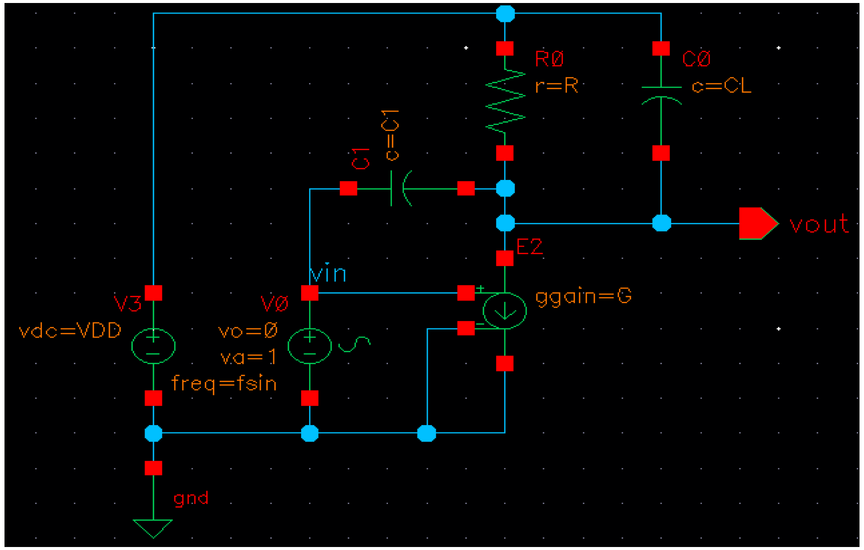
$$\frac{1 - k\,i\,\omega}{1 + k\,i\,\omega}\;\frac{1 + k\,i\,\omega}{1 - k\,i\,\omega}$$

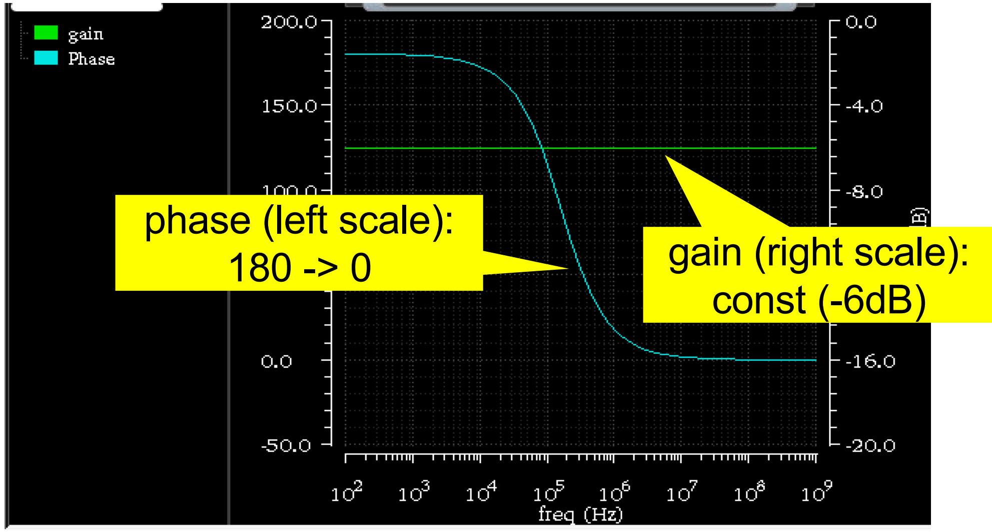
  which is 1.
  Therefore, the (absolute value) of the gain is constant!
- But the phase changes from inverting (180°) to non-inverting (0°). Funny!

RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

Solution 5

- We can simulate this with C1=CL=1pF, G=1uS -> R=500k yielding corners of 1MHz.





- This can also be seen in a transient sim. with a sine wave: