RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

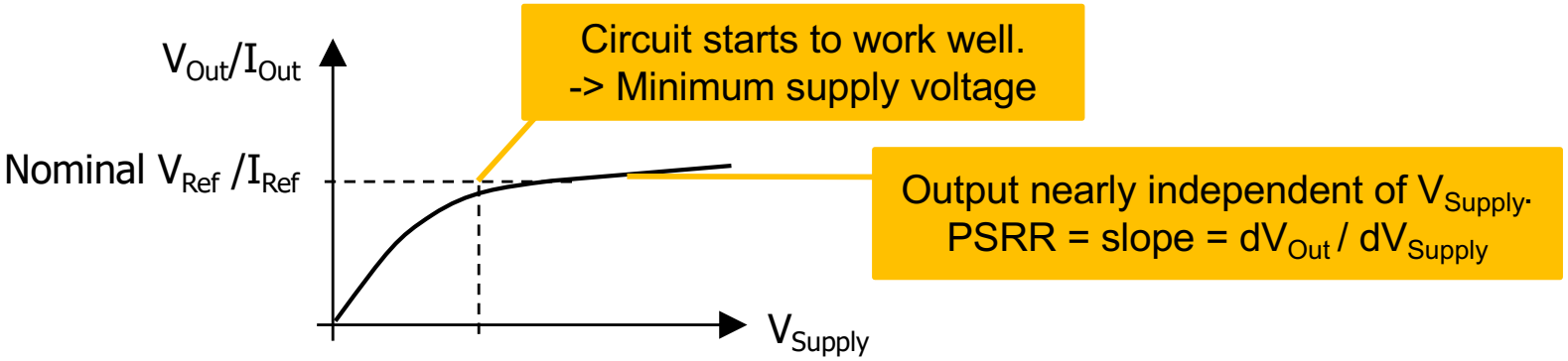
References

(only some very basic things)

P. Fischer, Heidelberg University

Goal

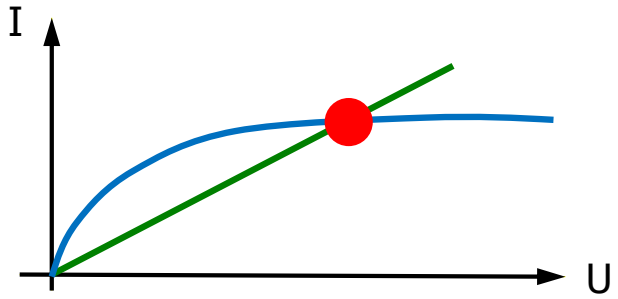
- To bias chips, we need a **reference** voltage or current
- This should be 'constant', i.e. mostly independent of
  - **P**rocess variations (Thresholds, resistor values,..)
  - Supply **V**oltage
  - **T**emperature
- Jargon: 'PVT independent'. Output of a circuit:



- To asses quality of a reference circuit, study
  - Power Supply Rejection Ratio (PSRR):
    relative change of V_{REF} vs relative change of V_{Supply}
  - Temperature Rejection (rel. change of V_{REF} per degree K)

Implementation

- Very common implementation principle:
  - Look for two different I(U) dependencies and find the intersection



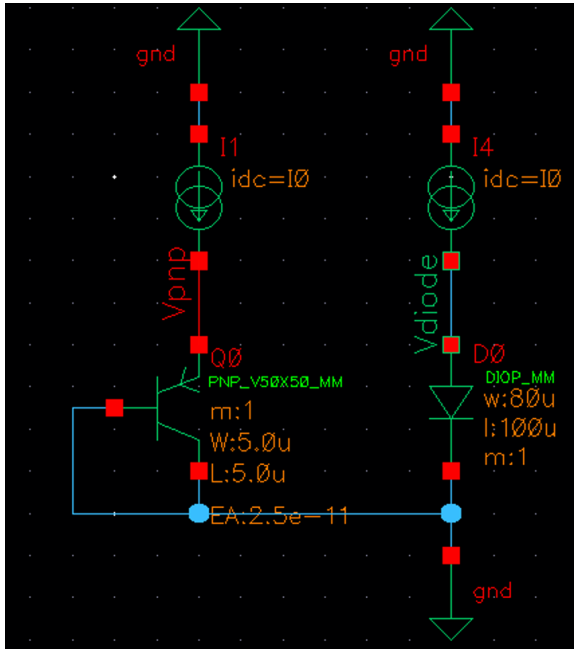
- There are normally 2 intersections!
  → Need **startup circuit** to avoid wrong operation point

Getting Rid of Temperature Dependence

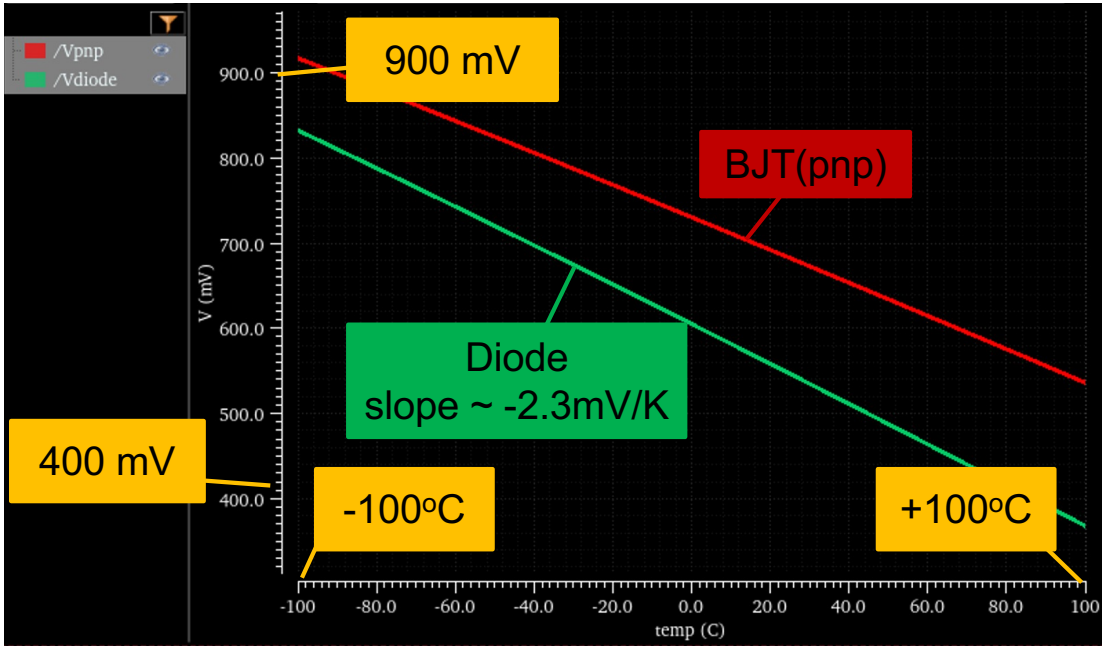
- Most component properties depend on temperature
- To obtain temperature independence, add two quantities with opposite temperature dependency
- Jargon:
  - PTAT = **P**roportional **T**o **A**bsolute **T**emperature
  - NTAT = **N**egative **T**o ..

Using a Diode (or BJT)

- Diode current $I_D \sim I_S(T)\,\mathrm{Exp}(V_D/U_{th})$ → $V_D = U_{th}\,\ln(I_D/I_S(T))$
  - $U_{TH} = kT/q$ ~25mV @ RT (PTAT!)
  - I_S depends on diode geometry etc.
    I_S also depends on temperature!
- The temperature dependency of $I_S(T)$ is quite strong so that ***overall***, the diode voltage (at constant current) ***drops*** with increasing temperature, i.e. it is **NTAT**:

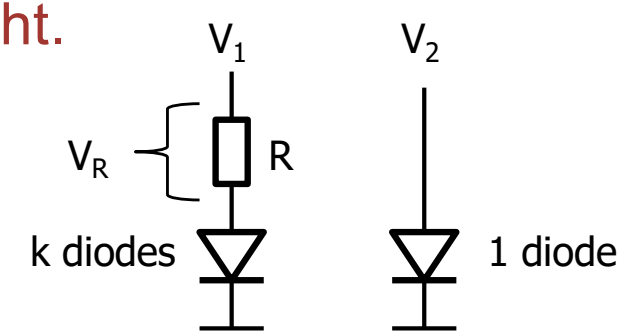


Sim @ 1uA



Typical Reference Topology

- Consider circuit shown right.
  Assume $V_1 == V_2$



- $V_R + U_{th} \ln(I_D/\mathbf{k}I_S) = V_1 == V_2 = U_{th} \ln(I_D/I_S)$
- $\rightarrow V_R = U_{th} \ln(I_D/I_S) - U_{th} \ln(I_D/\mathbf{k}I_S)$
  $= U_{th} [\ln(I_D/I_S) + \ln(\mathbf{k}I_S/I_D)]$

- $\rightarrow V_R = U_{th} \ln(k)$ (!) (if I_D is equal on both sides)
  - independent of diode parameters !
  - independent of supply voltage !

- BUT: U_{th} still depends on temperature… (PTAT)

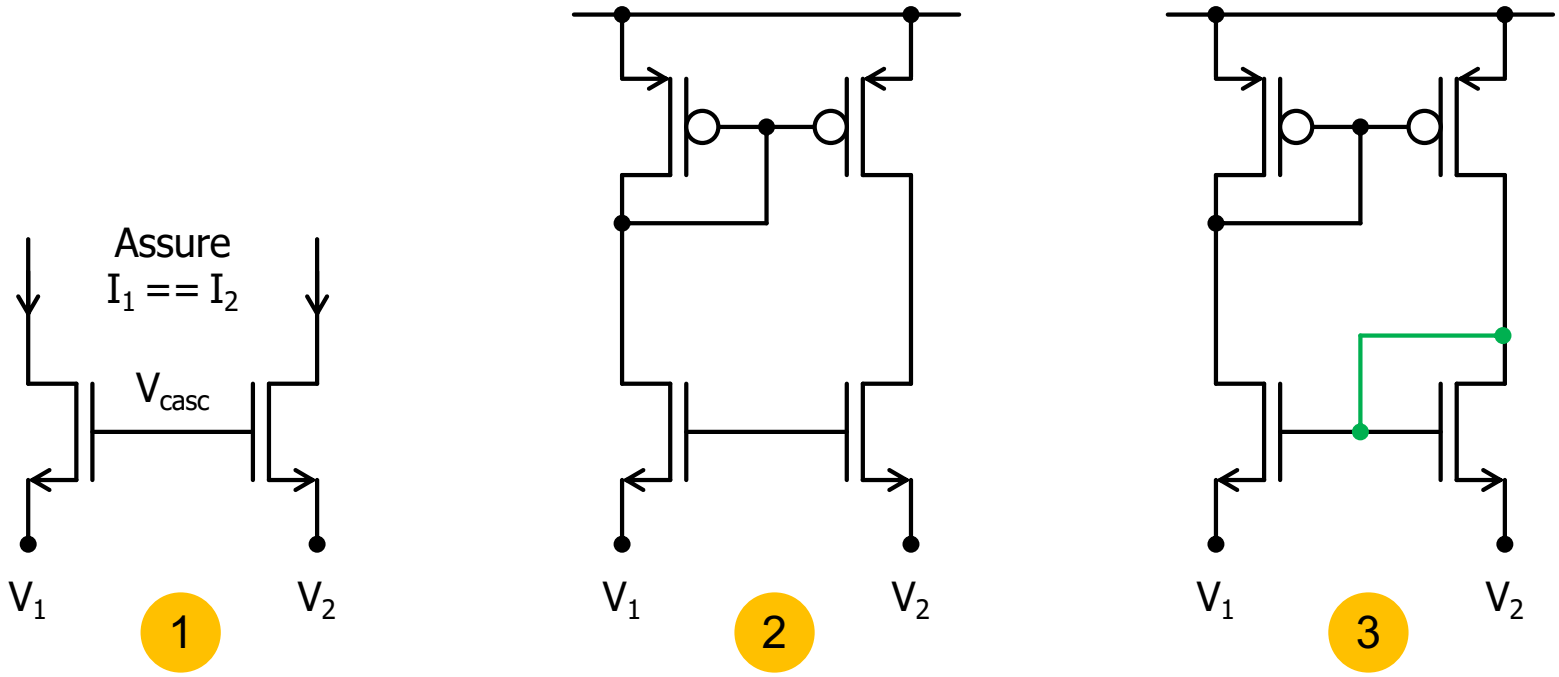
Diode / BJT

- Often a (parasitic) Bipolar Junction Transistor (BJT) is used because
  - It has a better model
  - It contains no parasitic elements
  - Forward biased diodes are normally not allowed

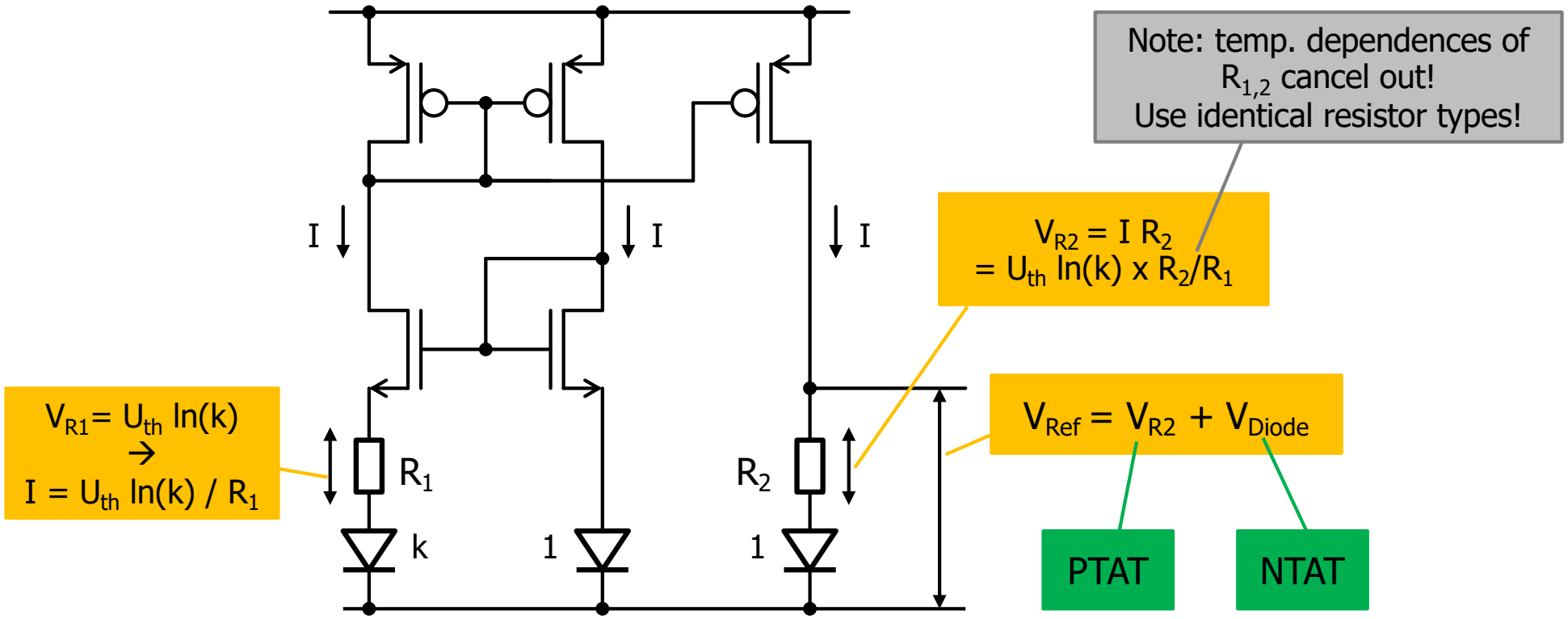
How to Achieve V_1 == V_2?

1. Use identical cascode MOS with
   - same gate voltages
   - identical currents (i.e. we must make sure I_1==I_2)
2. Use a mirror to assure I_1 == I_2
3. Use a Diode connection to find V_{casc}

   Why on the right side? (Hint: V_1==V_2 should not be fixed!)



Sample Implementation of a Reference



- Temperature **independence** is obtained if the temp-slopes of PTAT and NTAT just **cancel out**
- PTAT contribution can be tuned by adjusting e.g. R_2
- Requires good models to find right choice! Make test chips!

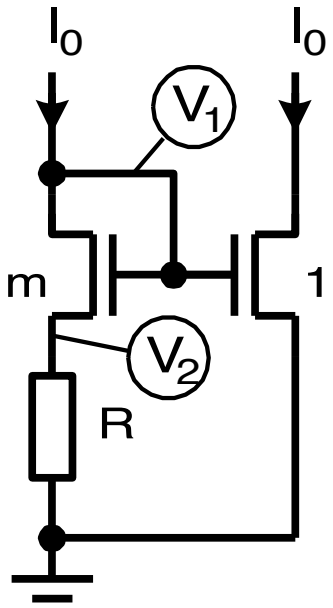
‘Curvature Correction’

- The Diode voltage is no perfectly linear NTAT
- The ‘quadratic’ term is not cancelled out with such a simple circuit (% effect)
- More advanced circuits try to correct the remaining ‘curvature’

Another Very Simple Reference

- This version 'uses the Cascode MOS as diodes'

MOS in weak inversion: $I_D = I_{DO} e^{\frac{V_G}{nU_{Th}}} e^{\frac{-V_S}{U_{Th}}}$



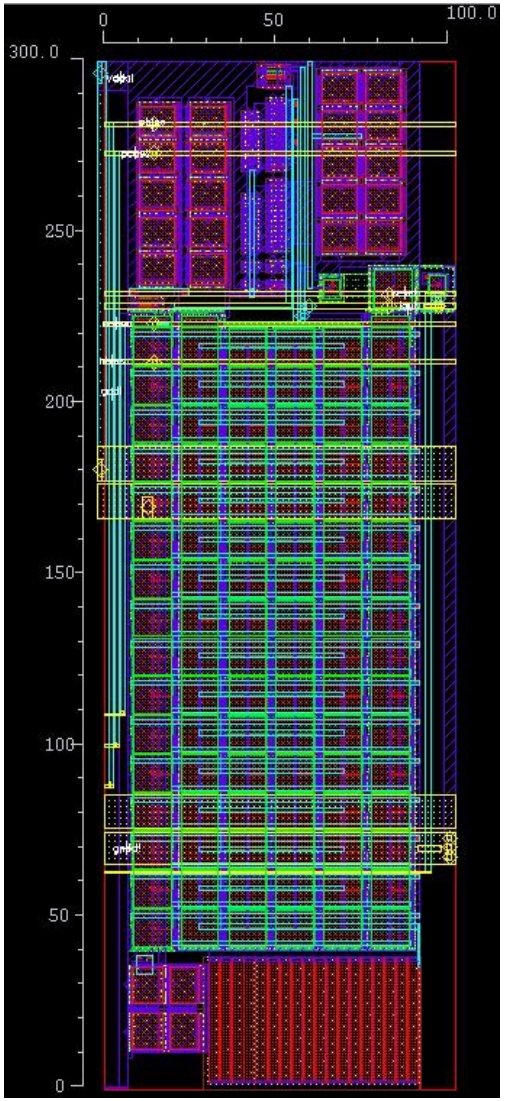
$$I_0 = mI_{DO} e^{\frac{V_1}{nU_{Th}}} e^{\frac{-V_2}{U_{Th}}}$$

$$I_0 = I_{DO} e^{\frac{V_1}{nU_{Th}}}$$

$$I_0 = V_2 / R$$

$$\Rightarrow I_0 = \frac{kT}{q} \frac{\ln m}{R}$$

Independent of technology parameters (but PTAT)!



Layout:
300µm x
100µm

Why Weak Inversion ?

Weak Inversion:

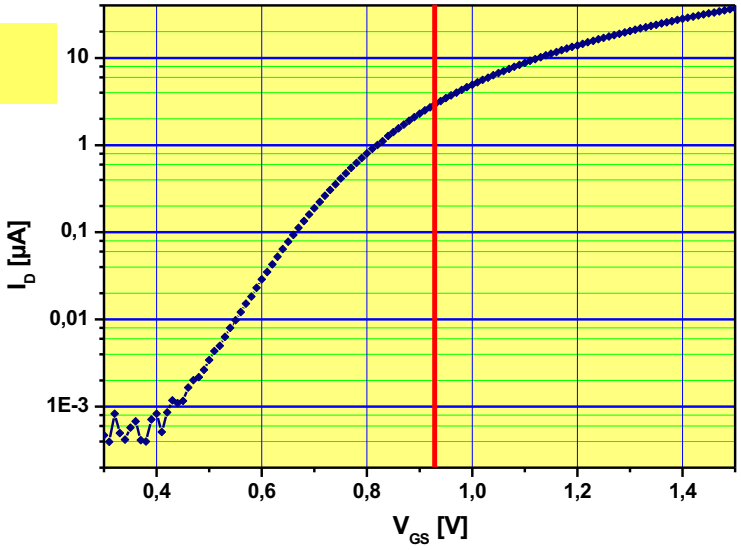
$$I_D = I_{DO}\, e^{\frac{V_G}{nU_{Th}}} e^{\frac{-V_S}{U_{Th}}}$$

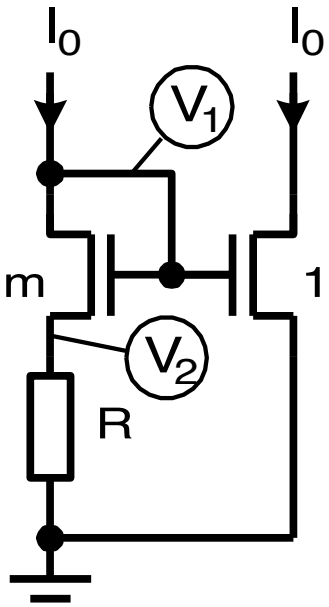
$$I_0 = m\, I_{DO}\, e^{\frac{V_1}{nU_{Th}}} e^{\frac{-V_2}{U_{Th}}}$$

$$I_0 = I_{DO}\, e^{\frac{V_1}{nU_{Th}}}$$

$$I_0 = V_2 / R$$

$$\Rightarrow V_2 = \frac{kT}{q} \ln m$$





Strong Inversion:

$$I_D = \frac{K}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$I_0 = m\frac{K}{2}\frac{W}{L}(V_1 - V_2 - V_T)^2$$

$$I_0 = \frac{K}{2}\frac{W}{L}(V_1 - V_T)^2$$

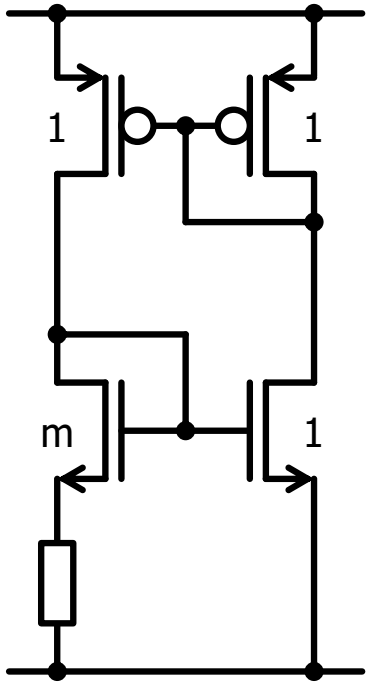
$$I_0 = V_2 / R$$

$$\Rightarrow V_2 = \frac{\sqrt{m} - 1}{m}\frac{1}{\frac{W}{L}\frac{K}{2}R}$$

Depends from Process Parameters

Minimal implementation

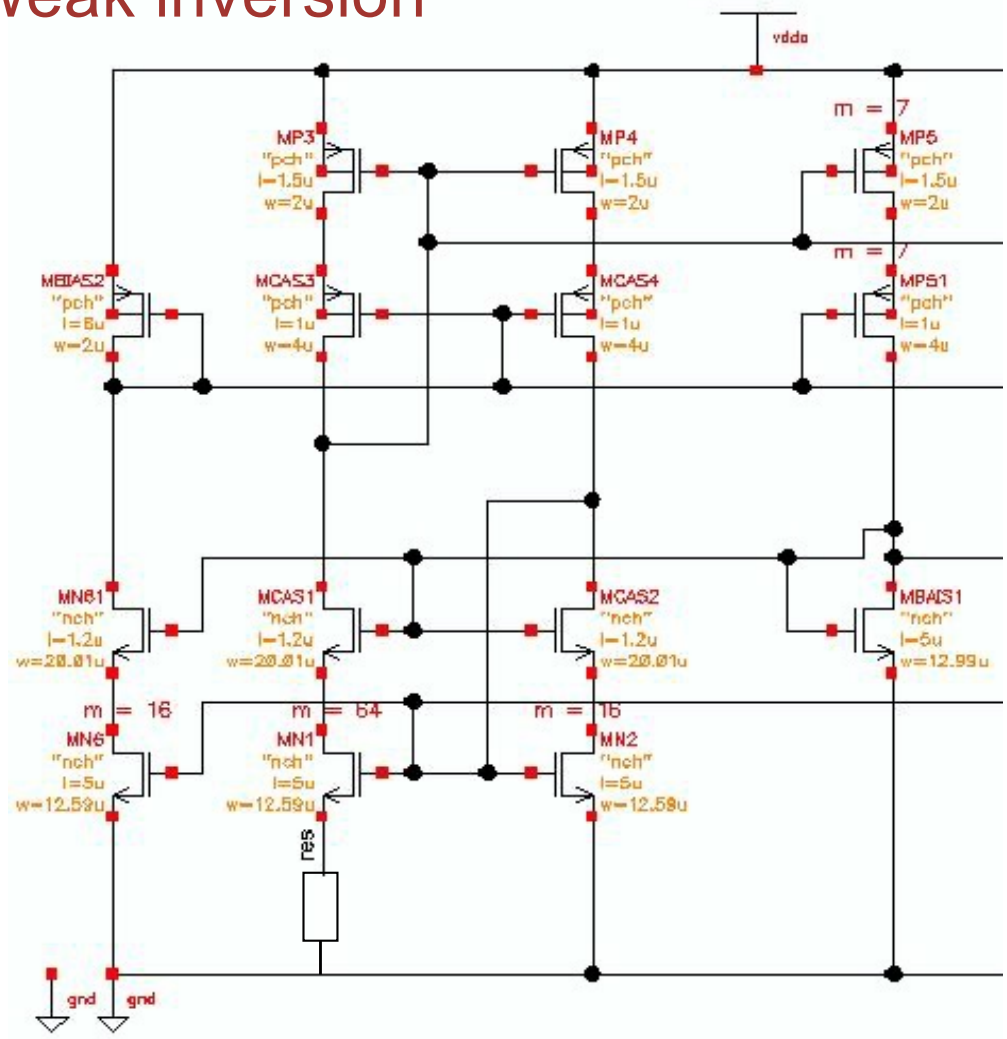
- Make currents equal with PMOS mirror:



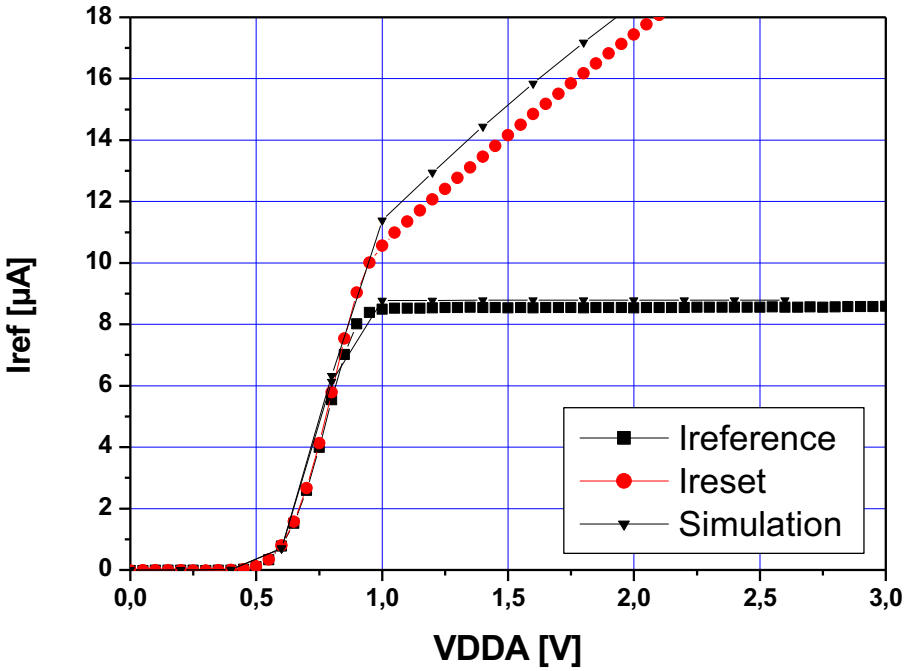
- Early effects in MOS lead to poor mirror ratios at changing supply voltage -> poor PSRR
- Can add Cascodes!

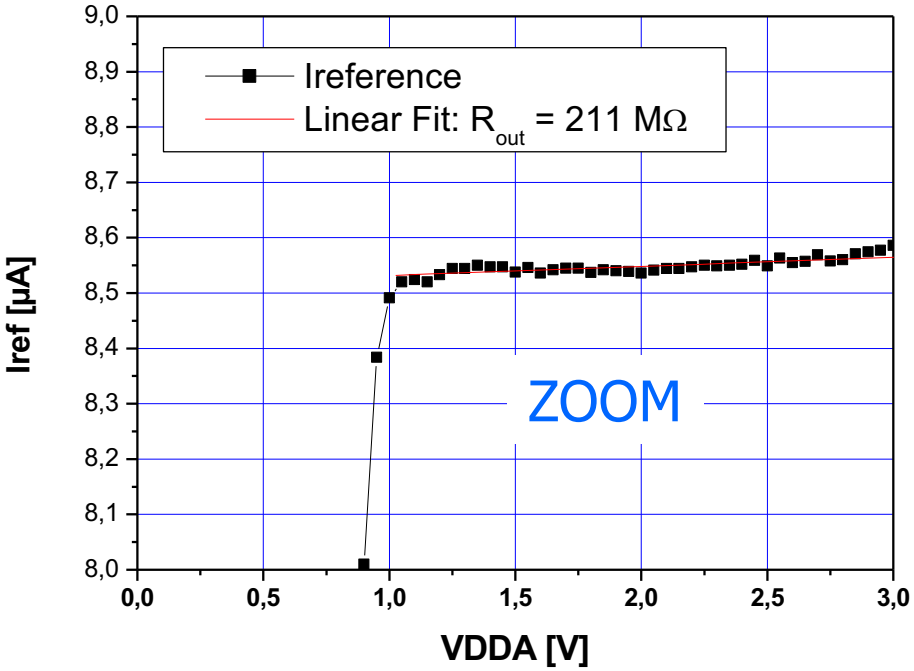
Detailed Schematic with Cascodes

- NMOS operate in weak inversion
- Resistor is P+ poly
- All MOS are cascoded using low voltage cascode circuits
- A reset signal forces node ‘res’ to ground
  -> current flows in circuit for guaranteed start



Measurements





- Very high output resistance of R_{out} > 200 MΩ
- Reference works at 1 V !